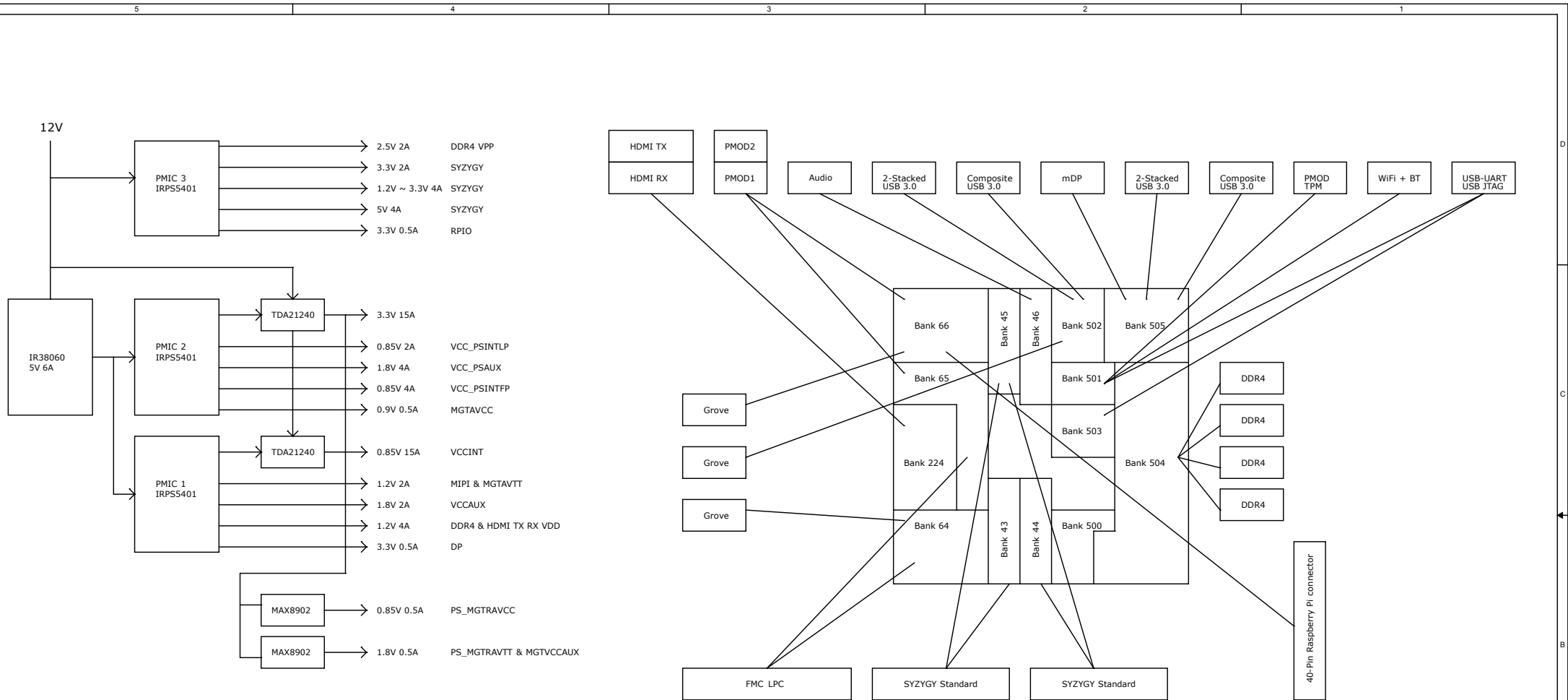


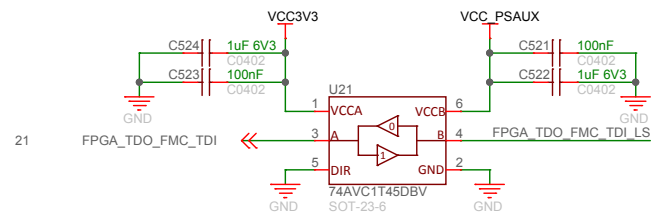
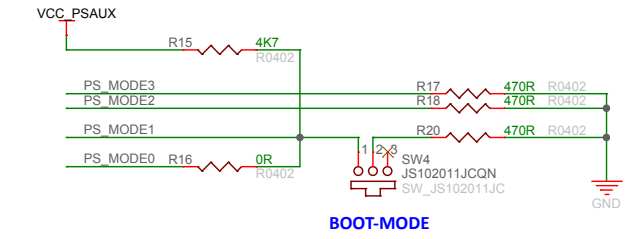
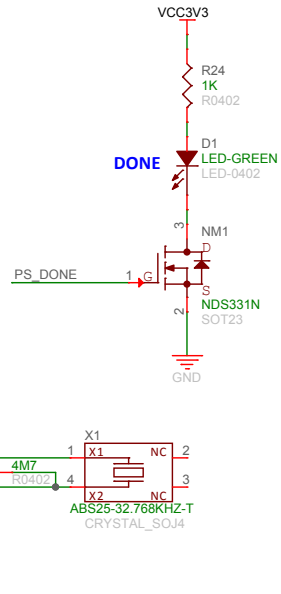
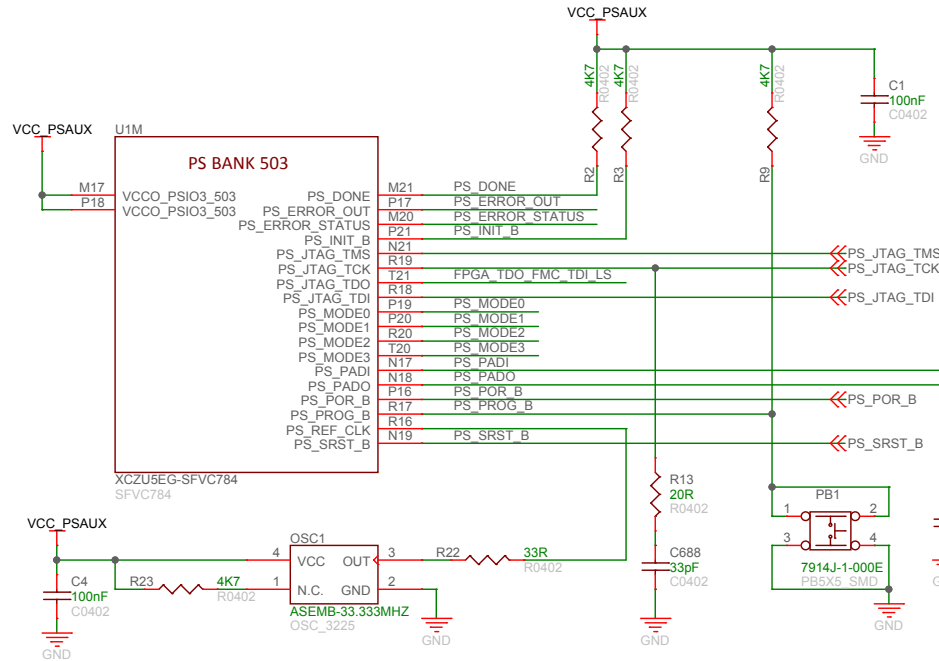
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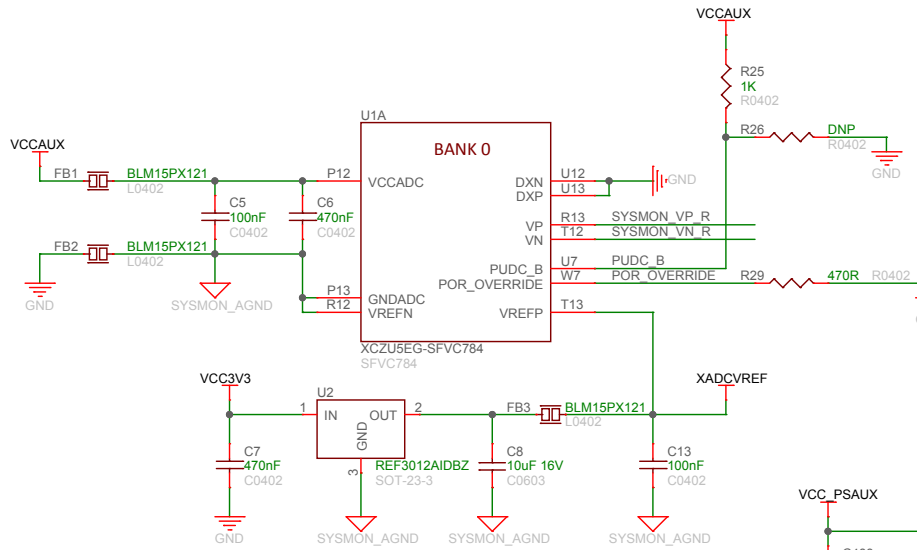
REVISION HISTORY

Rev.	DATE	CHANGE DETAILS
0.1	Feb, 18, 2019	First Release
0.2	Apr, 14, 2019	Update PCB Footprint Change SD level traslator
0.3	May, 06, 2019	Add SYZYGY PMIC Add Lithium Rechargeable Battery for RTC and BBRAM Add PMOD TPM Add Grove Interface
0.4	May, 18, 2019	FPGA & SYZYGY power change to Infineon solutions Remove J1 JTAG pin header Remove J7 WiFi debug pin header Remove J17 FT2232 UART pin header Remove U3 QSPI flash memory SW2~SW5 change P/N to J5102011JC GROVE power fix to 3.3V Power switch S1 change to vertical type
0.5	May, 21, 2019	Add PMIC Power Stage for VCCINT & VCC3V3 PS MODE setting SD0 default & JTAG only
1.0	May, 31, 2019	Update device speed Change LED BTN & SW Part Reference
1.1	Jun, 05, 2019	Update PMIC circuit, VIN_LDO range from 1.2V to 5.5V FPGA I/O SWAP
1.2	Jun, 08, 2019	USB2 change to USB3.0 Micro B type
1.3	Jun, 16, 2019	LPC GA0 GA1 wire to GND SYGYZY VIO power EN wire to FPGA MIO36
1.4	Jun, 17, 2019	FMC_LPC_PRSNT_M2C_B wire to FPGA MIO6 Si5319 change to Si5324
2.0	Jun, 28, 2019	FPGA I/O adjust for FMC full connection Two SYGYZY shared 3.3V but VIO independent Add DDR4 2.5V VCC_PSPDLL wired to VCC1V2 PMIC FB change to 0R R534 change to 5K62, R486 change to 1K4, add FB67 Add PS_DDR_BG0 pull up R551
2.1	Sep, 22, 2019	Modify LEDs SWs BTNs to FPGA pins assigment. Swap FMC to FPGA pin pairs LPC_LA31 ~ LPC_LA32 Add PB5 to FPGA pin H2 forURST_B
2.2	Oct, 05, 2019	Connect CHIP_EN (pin 19) of U36 chip to MIO4 Connect RESET_N (pin 7) of U36 chip to MIO5 Connect U47 (PMIC1) channel D VCCO_PSDDR to U27 (HDMI TX) and U30 (HDMI RX) 1.2V rail Remove connection MIO 76 and MIO 77 to U59. Connect MIO0 to U59 pin 4 and MIO1 to U59 pin 5
2.3	Oct, 16, 2019	Fixed USB 3.0 micro-B TX & RX pinout. Change MGTRAVTT power up after MGTA VTT.
2.4	Oct, 25, 2019	Fixed some lebel error
2.5	Nov, 05, 2019	U24 DP TVS change to RClamp0524P Change power sequence PSINTFP --> MGTRAVCC --> MGTRAVTT
2.6	Nov, 08, 2019	FMC_LPC_GBTCLK0_M2C_P/N swap to Si5324 CLKIN_2
2.7	Nov, 12, 2019	FMC GBT Clocks add ac capacitors and resistor.
2.8	Nov, 23, 2019	Change USB1 P/N to 105017-0001 Change FT4232 to FT2232 and reset pull-up to VBUS Add a fan power connector
2.9	Nov, 26, 2019	Change Micro USB-AB P/N to ZX62D-AB-5P8(30) D37 & D38 pins swap for PCB layout
2.A	Nov, 28, 2019	Modify text labels
2.B	Dec, 04, 2019	Change FT2232 reset pull-up back to VCCIO
3.0	Jan, 21, 2020	Add zener diode between PMIC and Power Stage PWM Add divider resistor in PMIC LDO SYZYGY PMIC I2C change to PMBUS I2C PMIC VIN_A change to 12V for match with power stage VIN Modify PMIC components Spec.
3.1	Feb, 05, 2020	IR38060 Pin 20 P1V8 bypass with a capacitor to LGND.
3.2	Feb, 13, 2020	U47 U48 VIN_B ~ VIN_D change to 12V
3.3	Feb, 17, 2020	R562, R563 change to 499R
3.4	Feb, 25, 2020	R564 change to 10K
3.5	Jun, 12, 2020	LED D2 D3 change to white color
3.6	Jul, 09, 2020	U59, U60, U61 change to TXS0102DCU
3.7	Jul, 10, 2020	U37~U39 TXS0108E change to TXB0108RGY
3.8	Aug, 24, 2020	

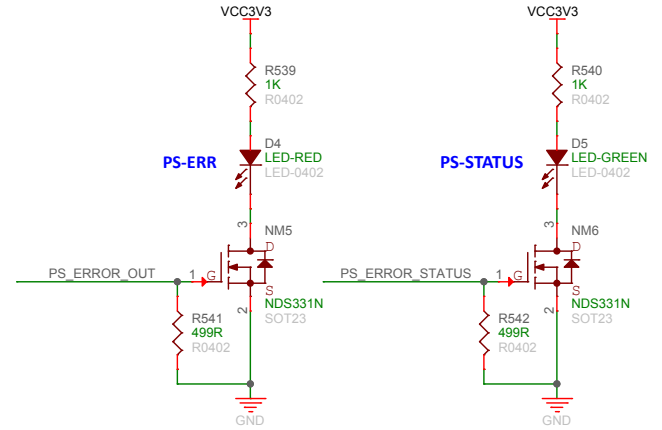
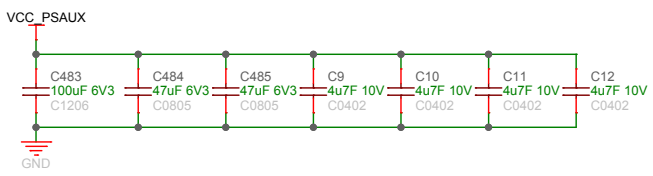
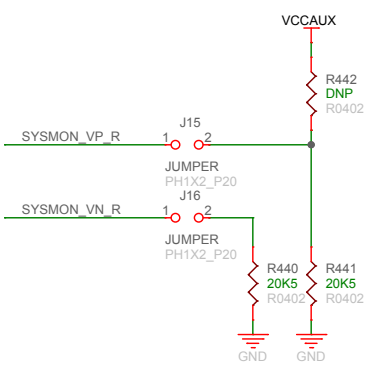




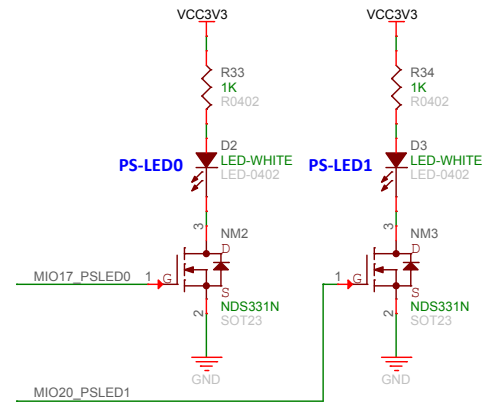
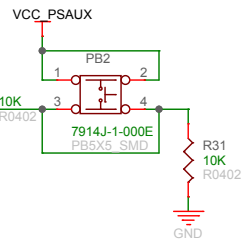
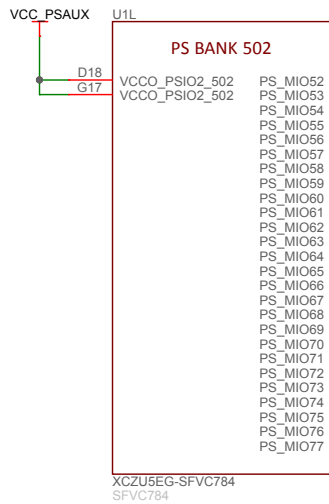
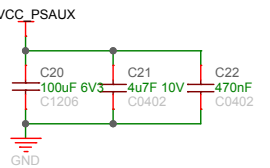
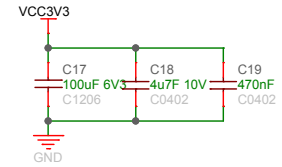
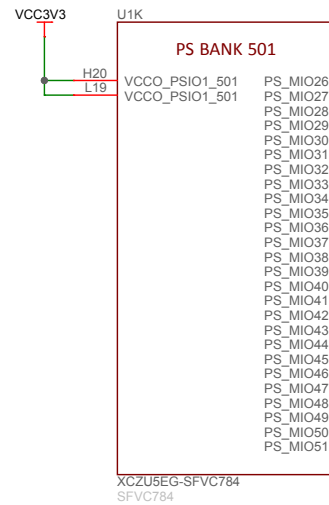
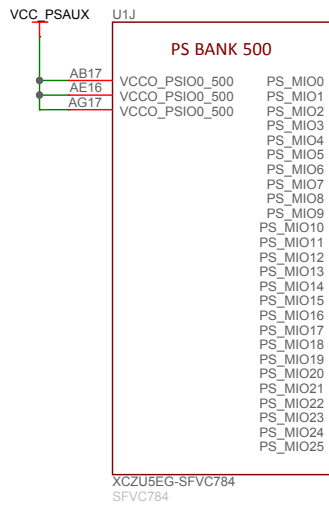
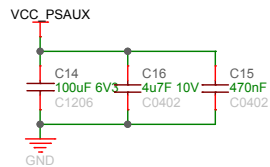
Boot Mode	MODE PIN[3:0]	Description
JTAG	0000	Dedicated PS interface
SD0	0011	Supports SD 2.0



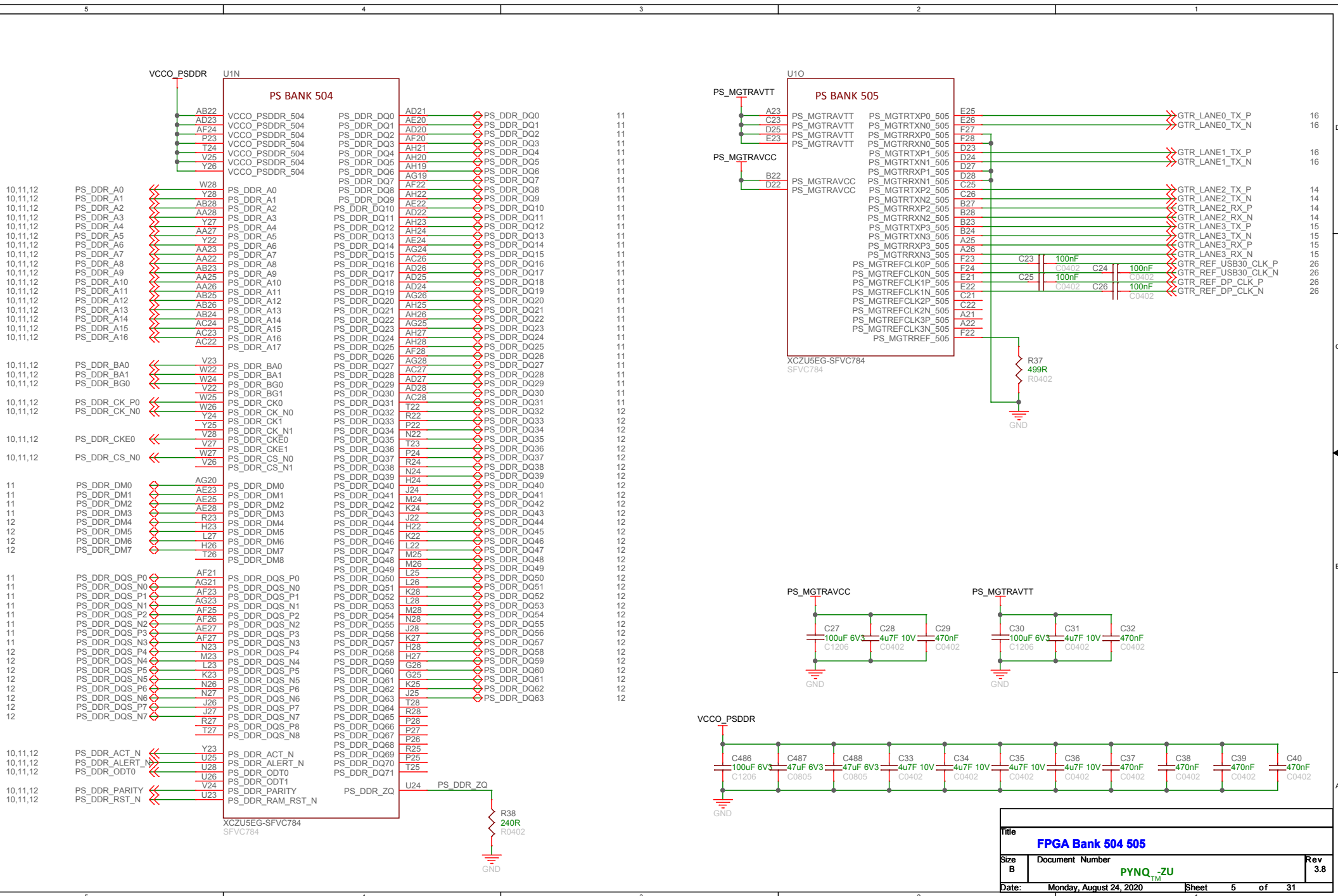
SYSMON I2C Address Jumpers



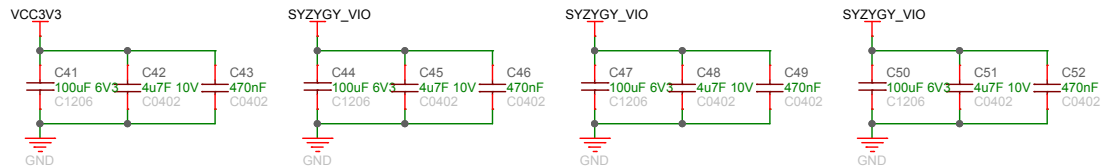
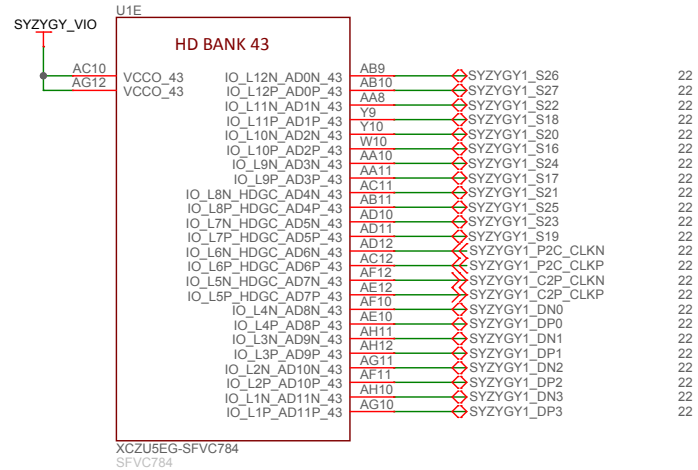
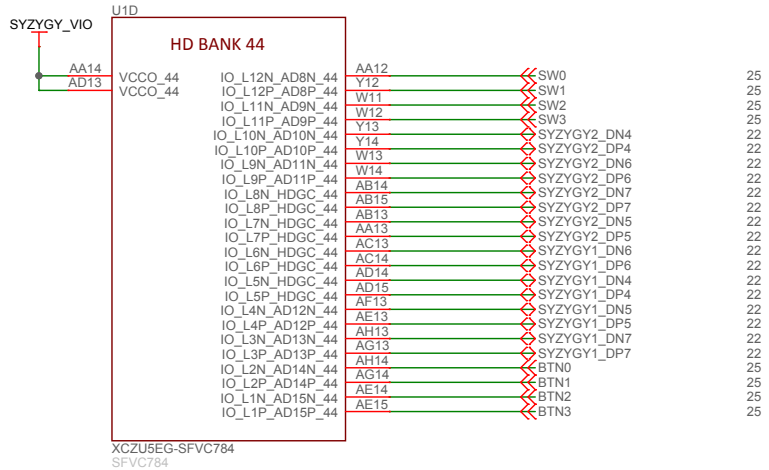
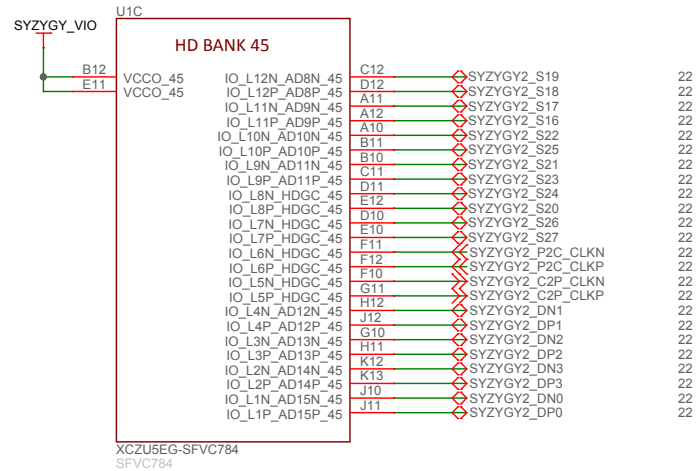
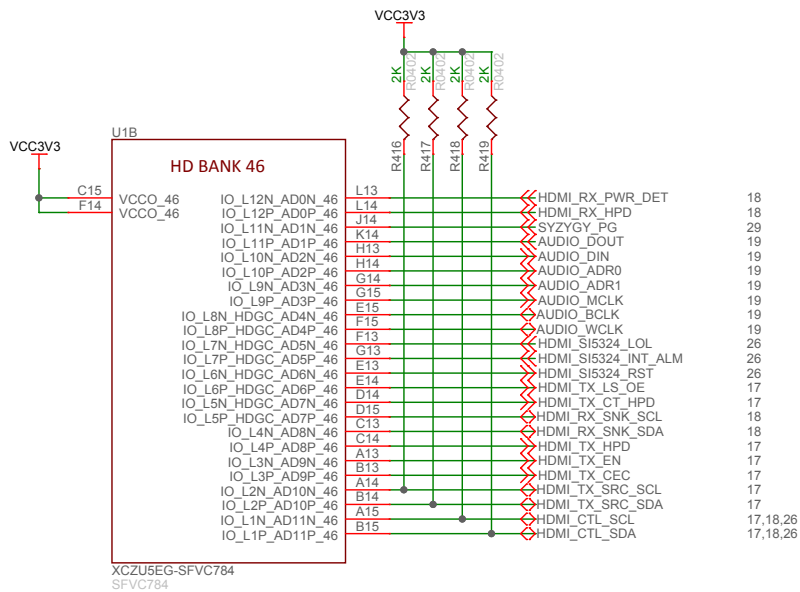
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Size	Document Number	Rev	
B	PYNQ_ZU	3.8	
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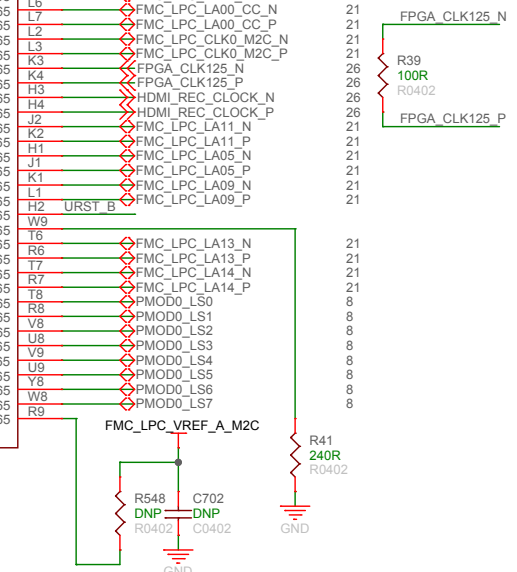
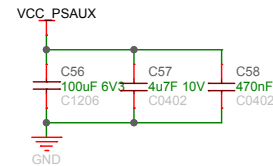
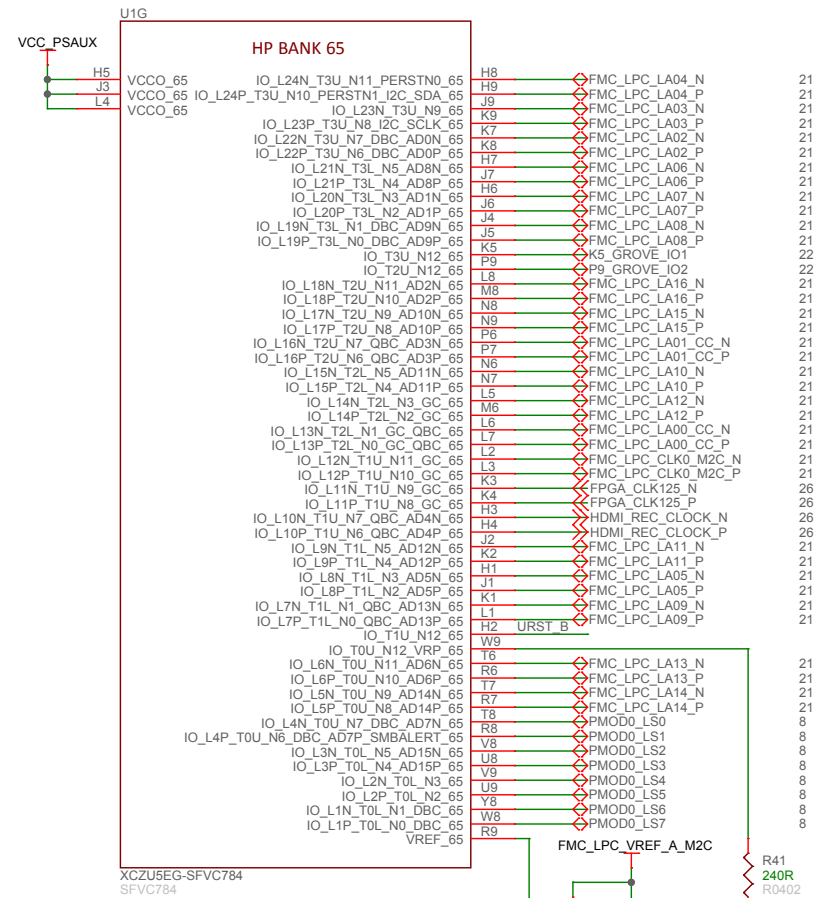
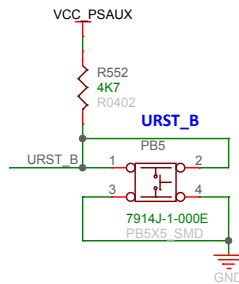
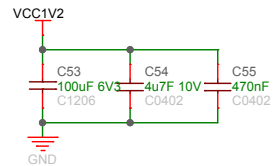
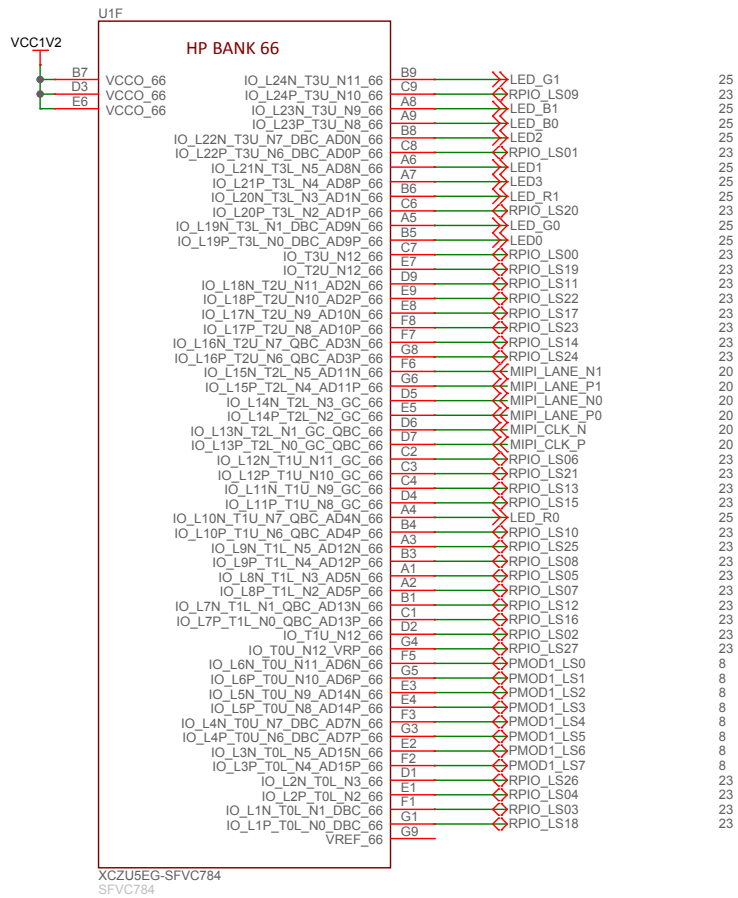
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Size	Document Number	Rev	
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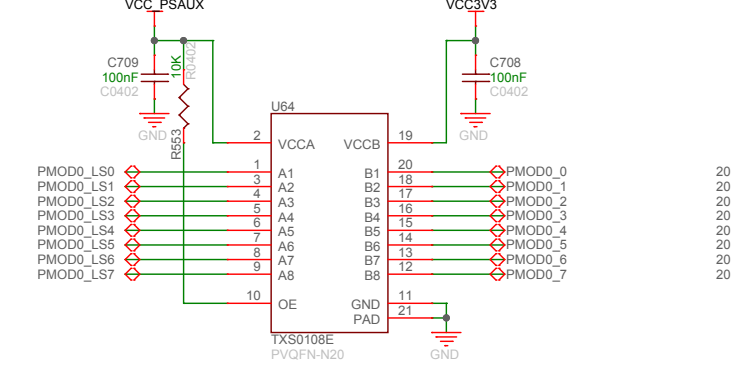
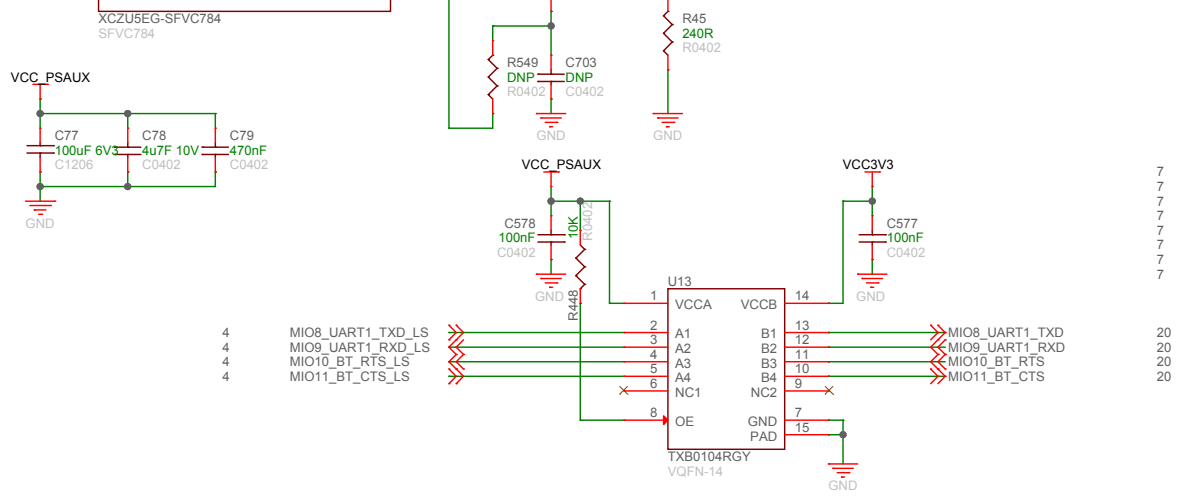
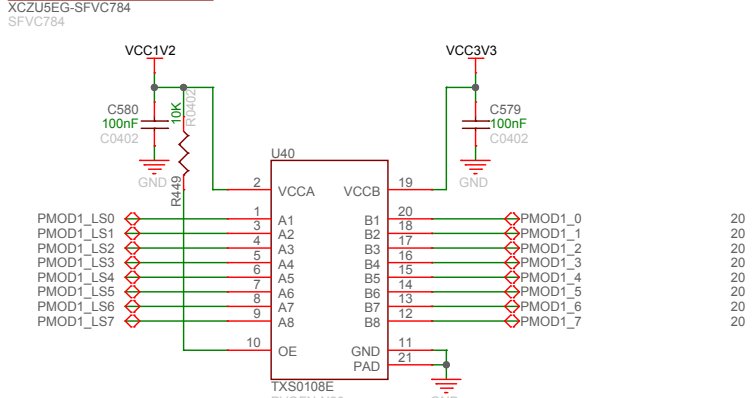
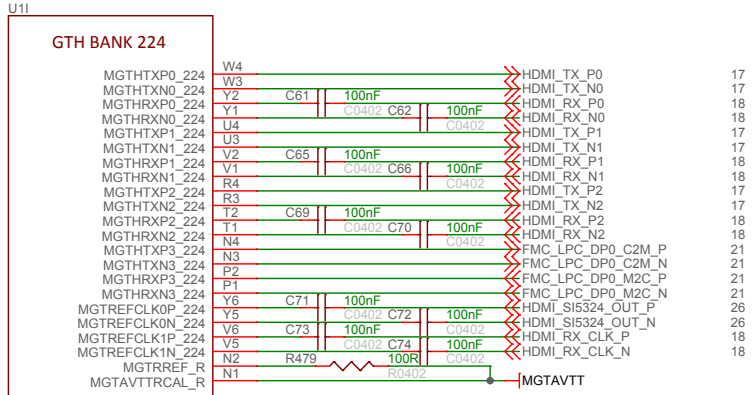
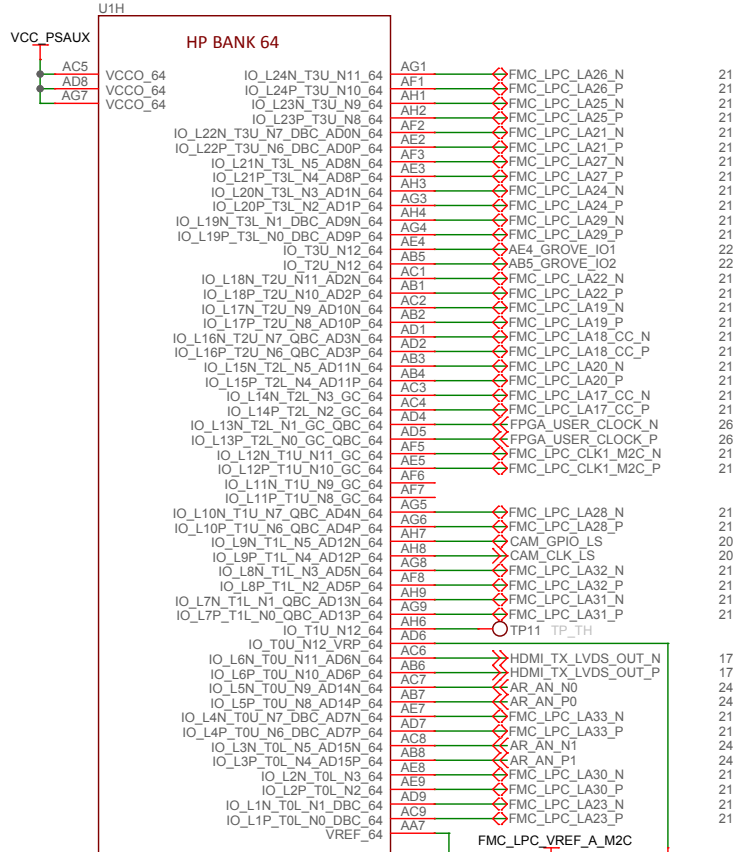
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Size	Document Number	Rev	
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Title		
<b>FPGA Bank 43 44 45 46</b>		
Size	Document Number	Rev
B	<b>PYNQ<sub>™</sub>-ZU</b>	3.8
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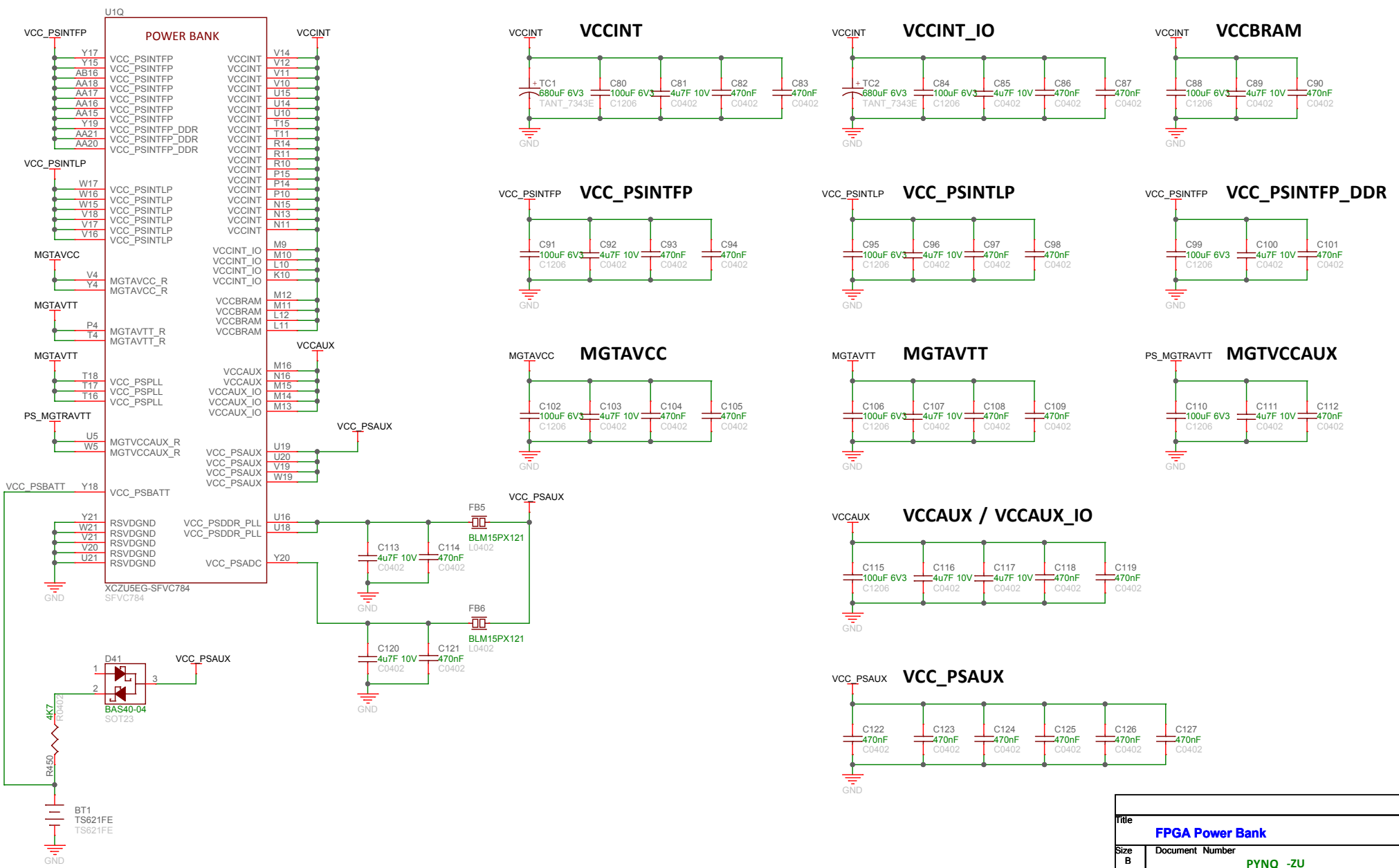


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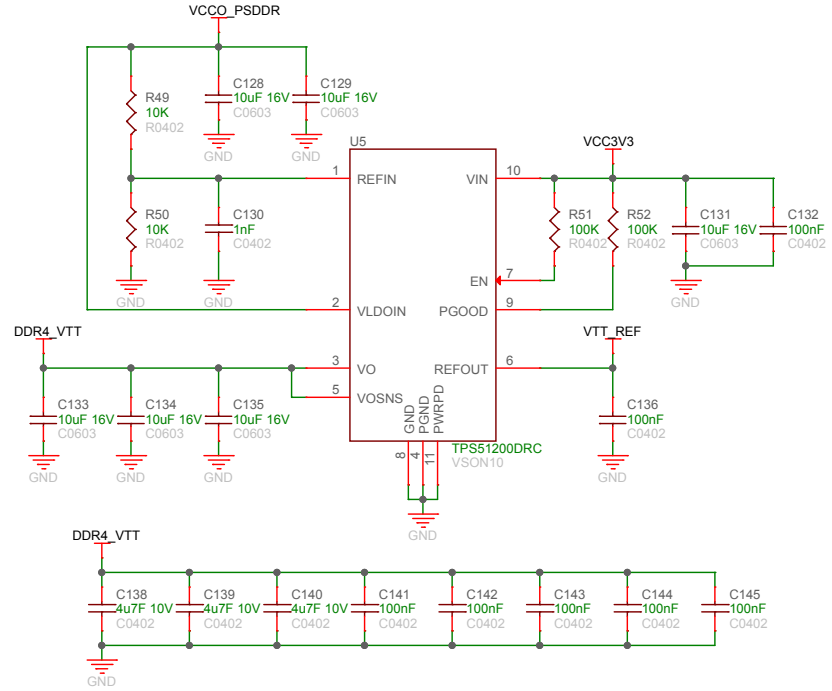
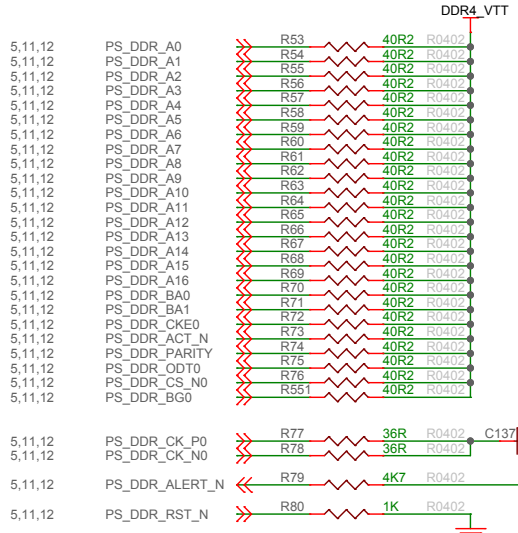
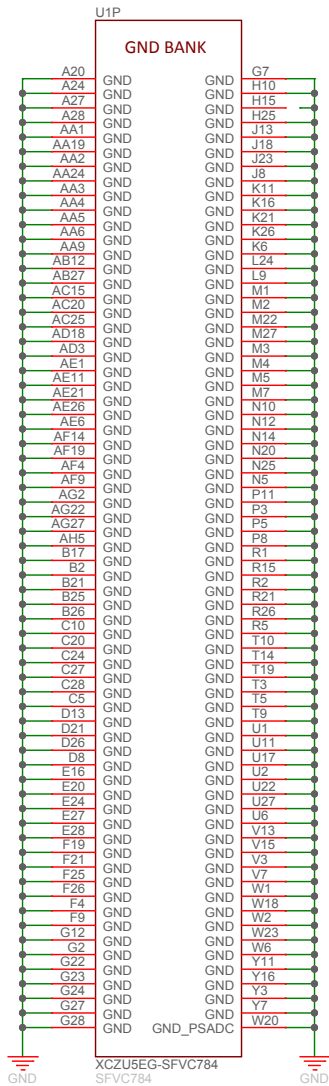


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Size	Document Number	Rev
B	PYNQ_ZU	3.8
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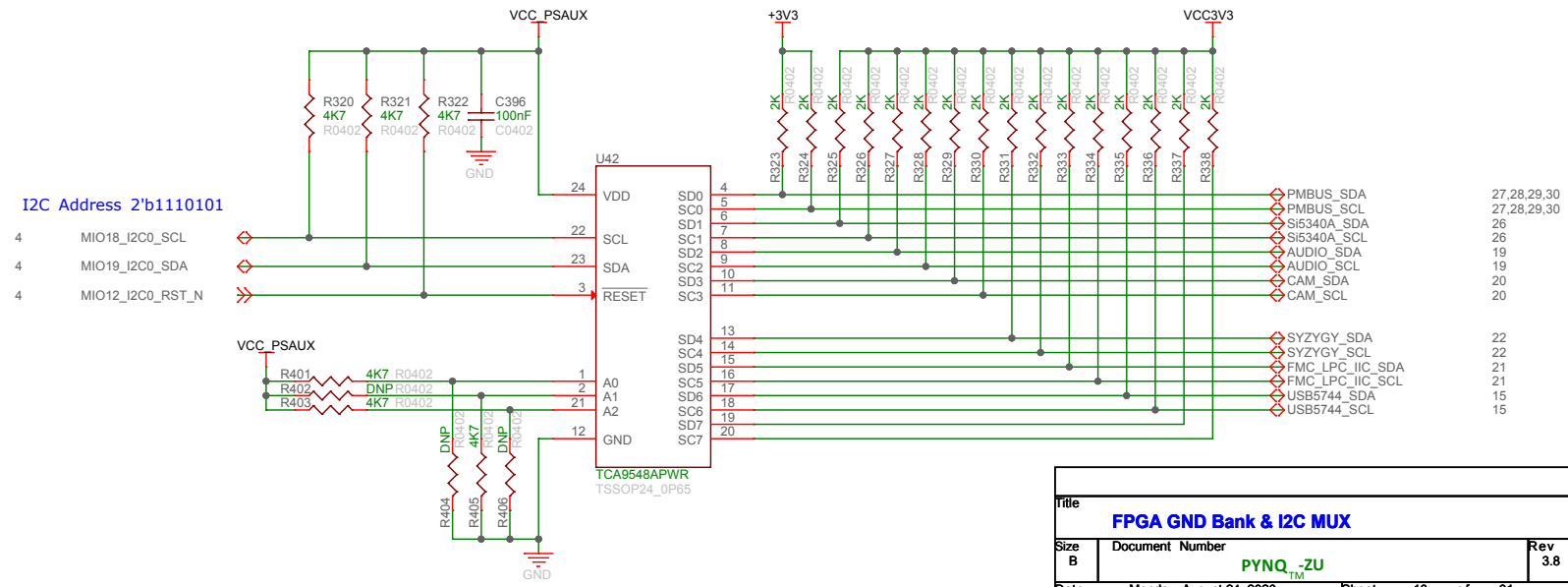




Title		
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Size	Document Number	Rev
B	PYNQ-ZU	3.8
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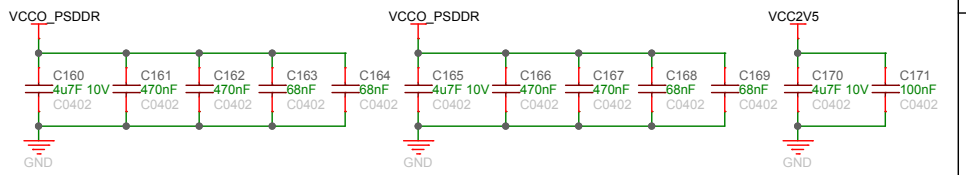
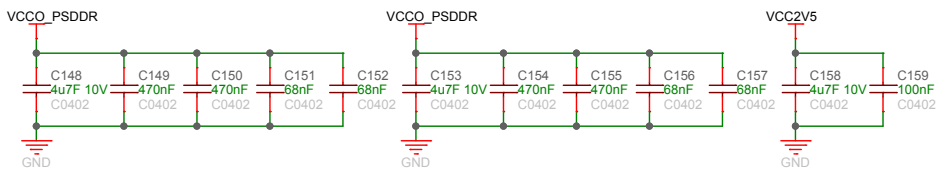
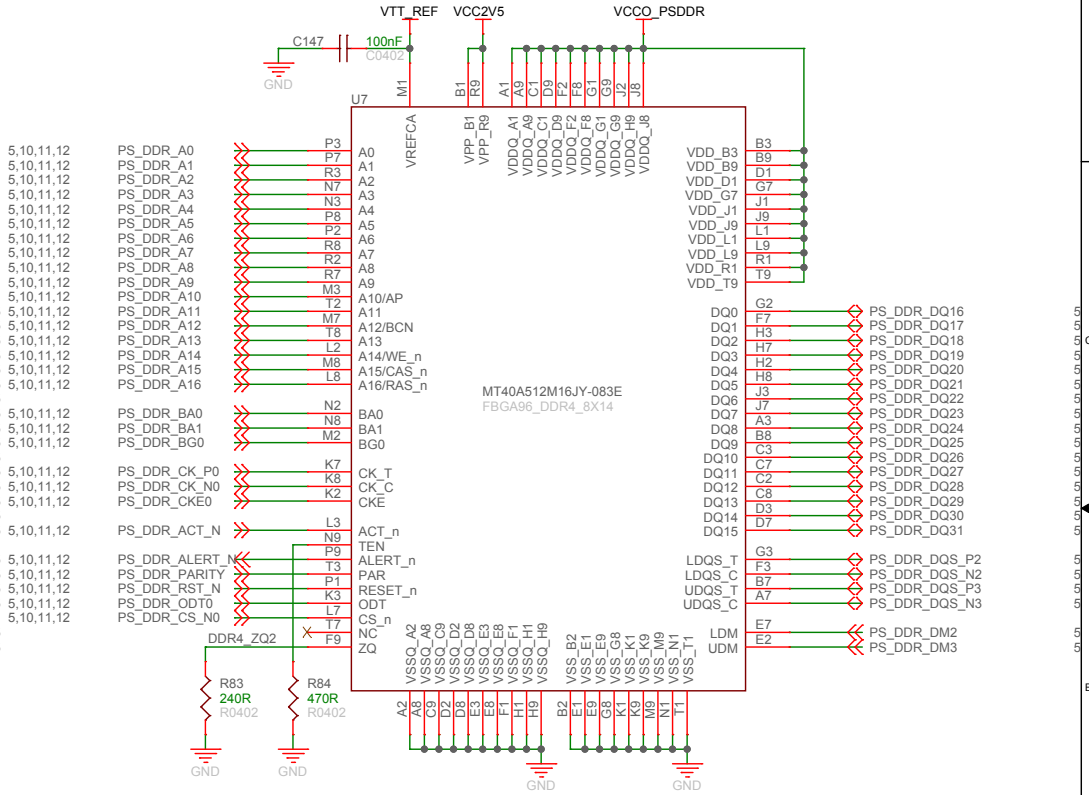
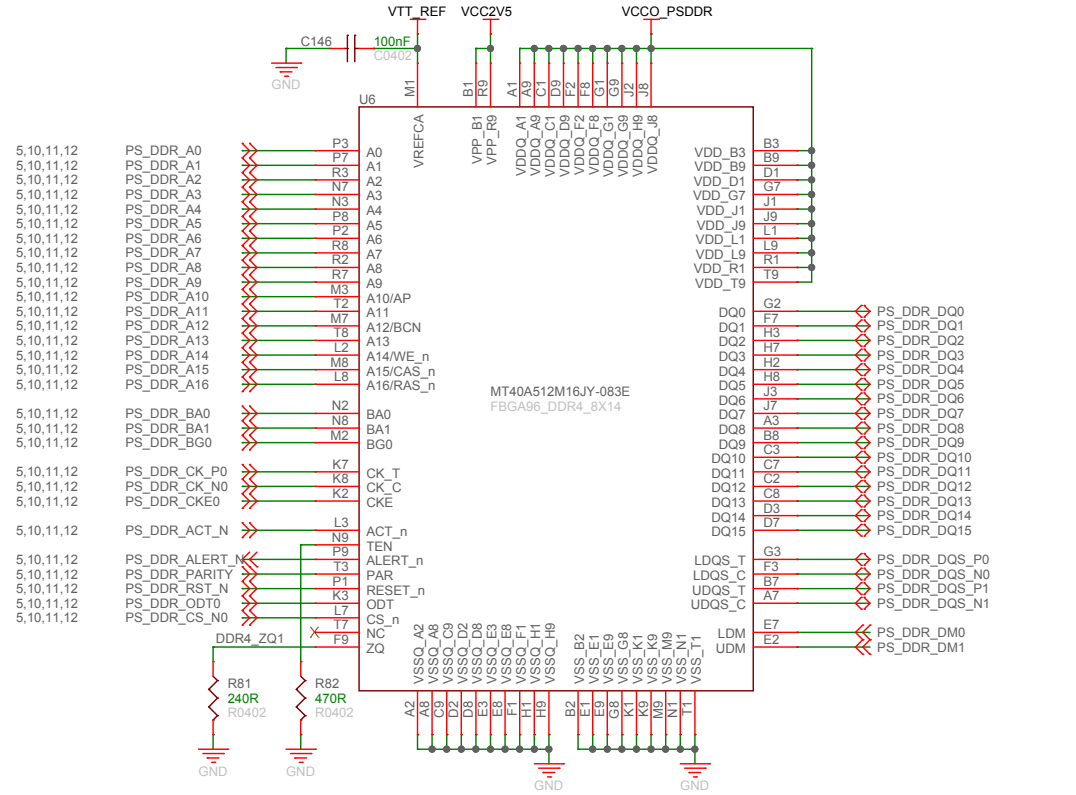
### PS I2C MUX



Title		
<b>FPGA GND Bank &amp; I2C MUX</b>		
Size	Document Number	Rev
B	PYNQ_ZU	3.8
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# DDR4 64b 1/2

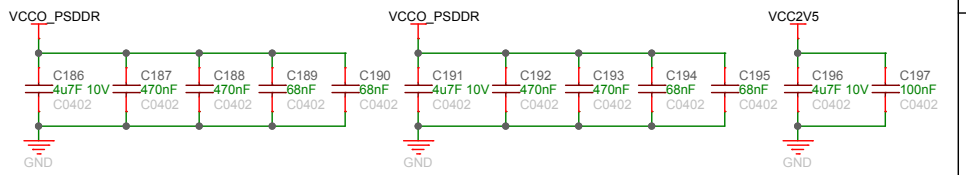
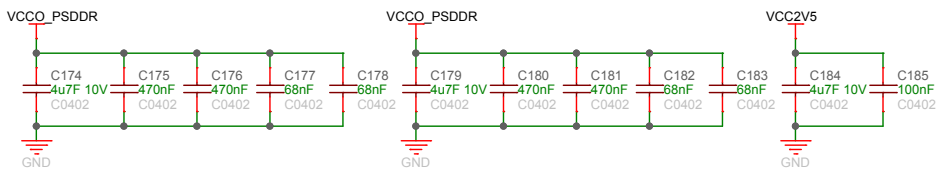
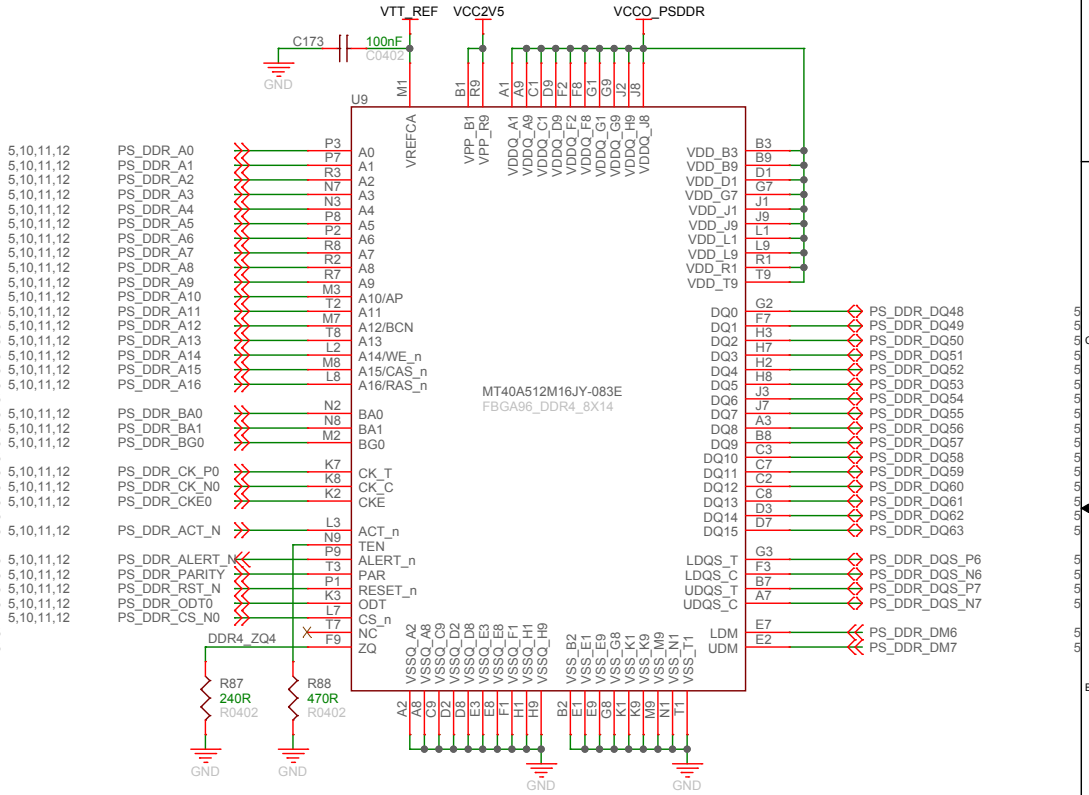
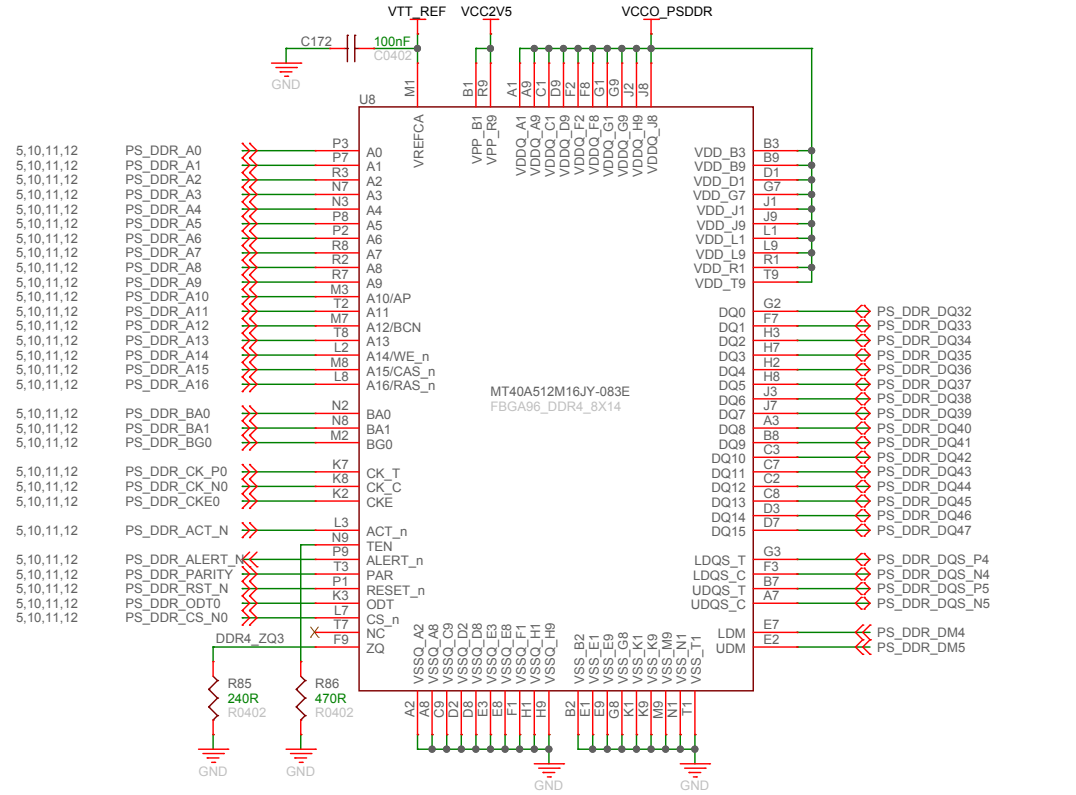
DDR4 2133MHz



Title		
DDR4 64b 1/2		
Size	Document Number	Rev
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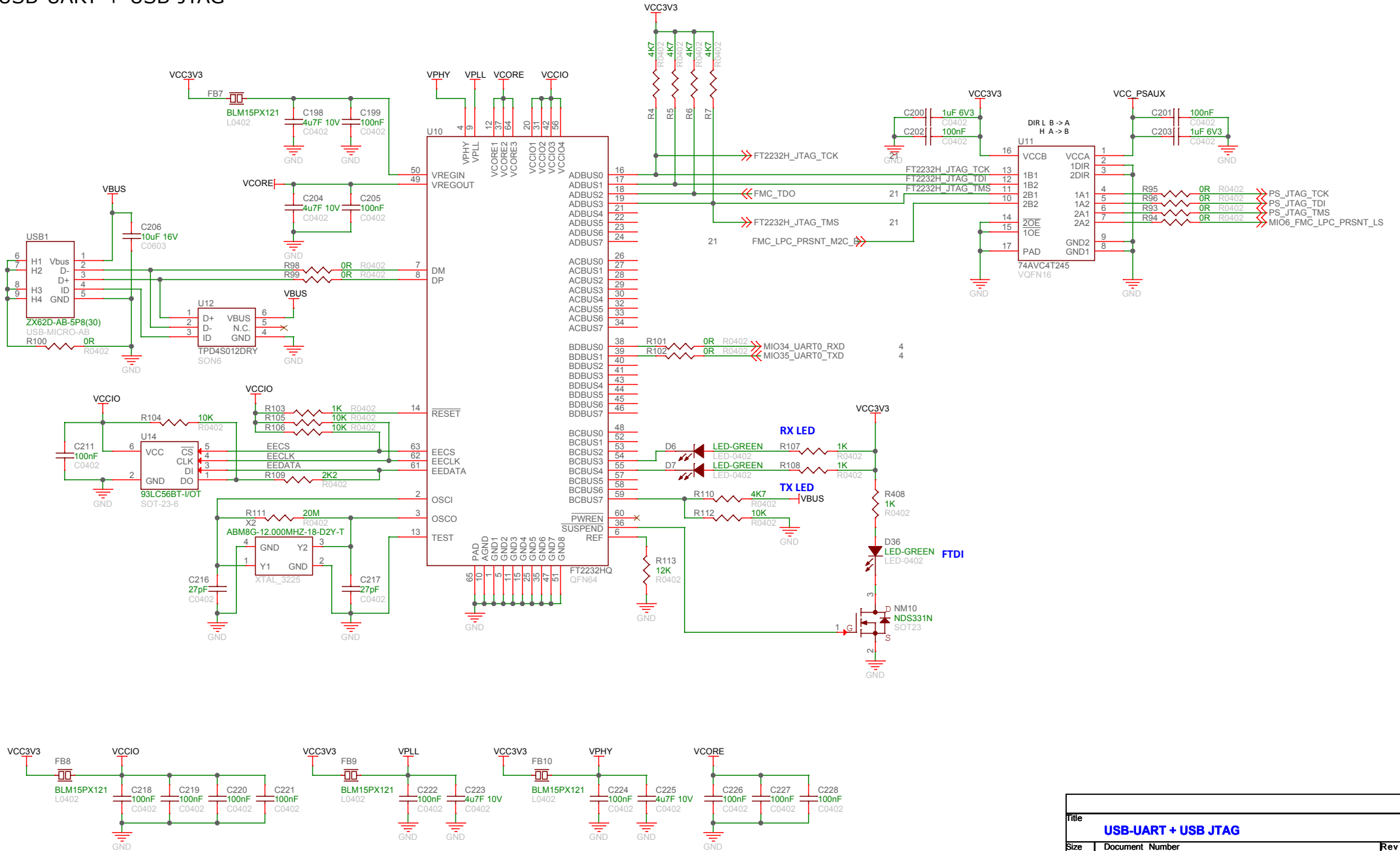
# DDR4 64b 2/2

DDR4 2133MHz



Title		
DDR4 64b 2/2		
Size	Document Number	Rev
B	PYNQ_ZU	3.8
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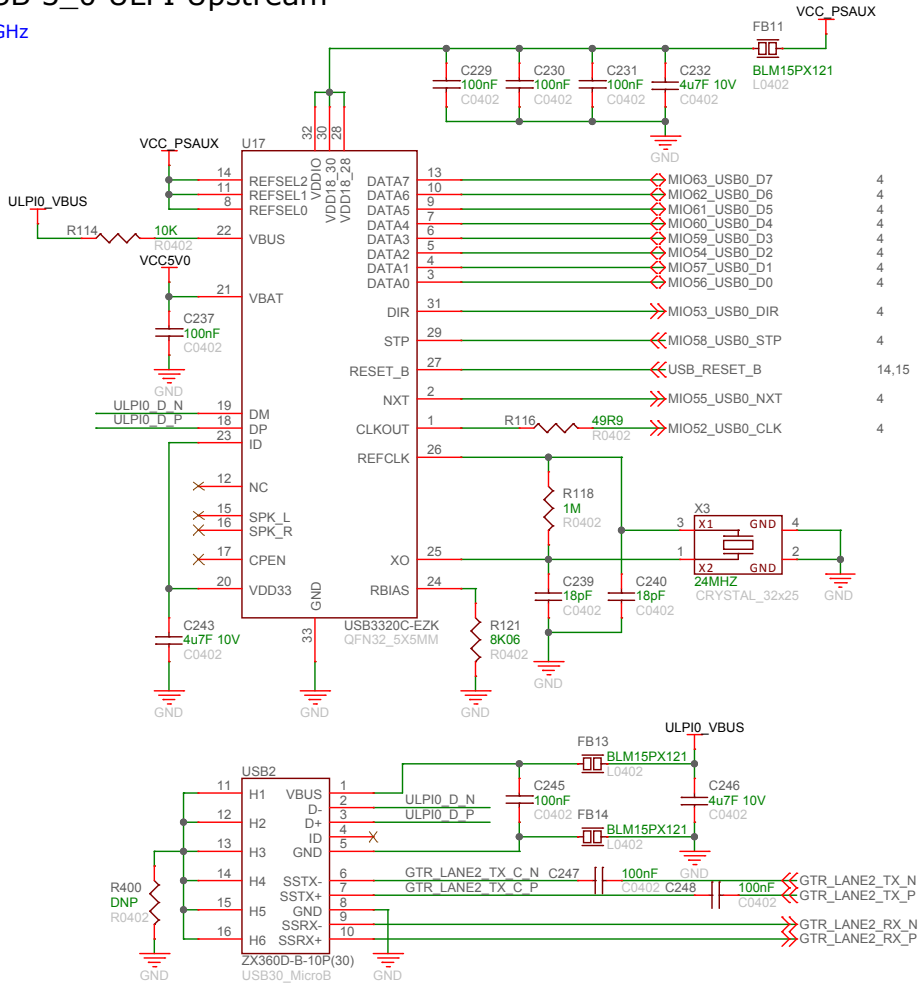
# USB-UART + USB JTAG



Title		<b>USB-UART + USB JTAG</b>	
Size	Document Number	PYNQ <sub>™</sub> -ZU	
B			Rev 3.8
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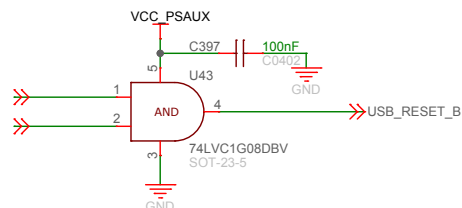
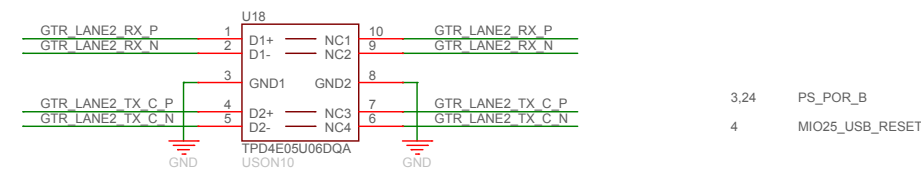
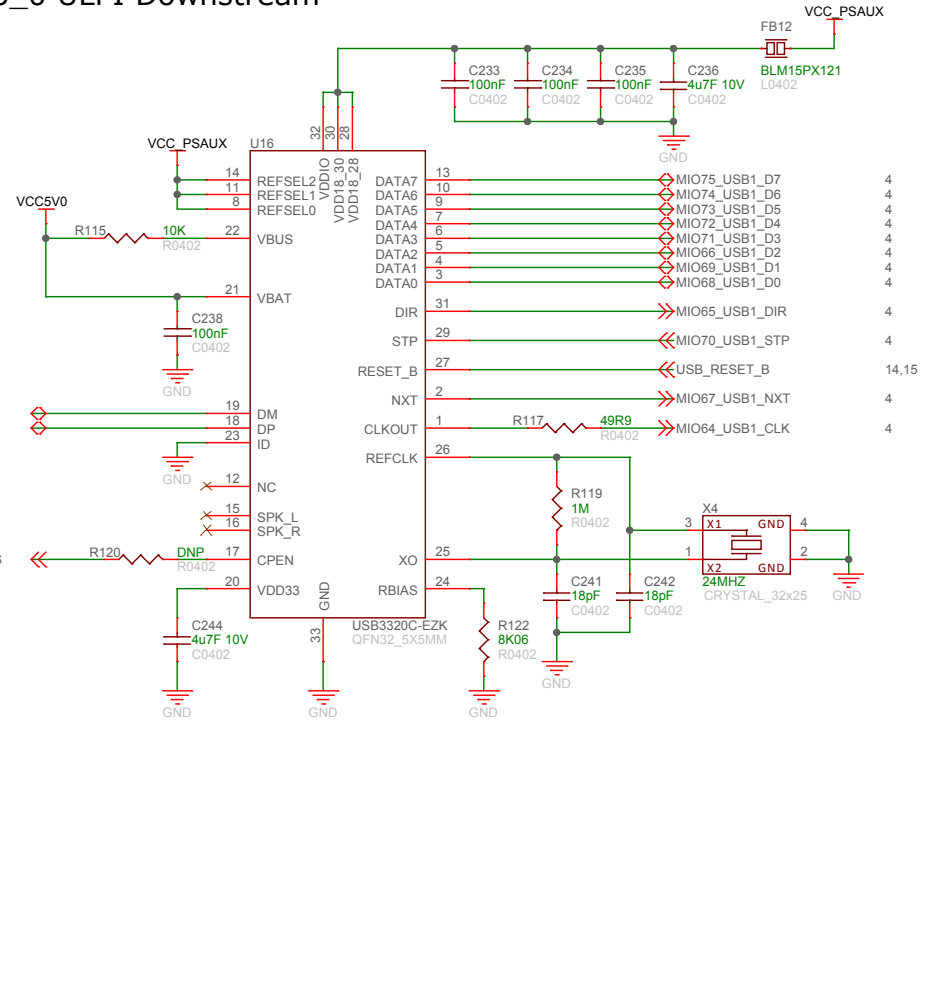
# PS USB 3\_0 ULPI Upstream

USB 5GHz



# PS USB 3\_0 ULPI Downstream

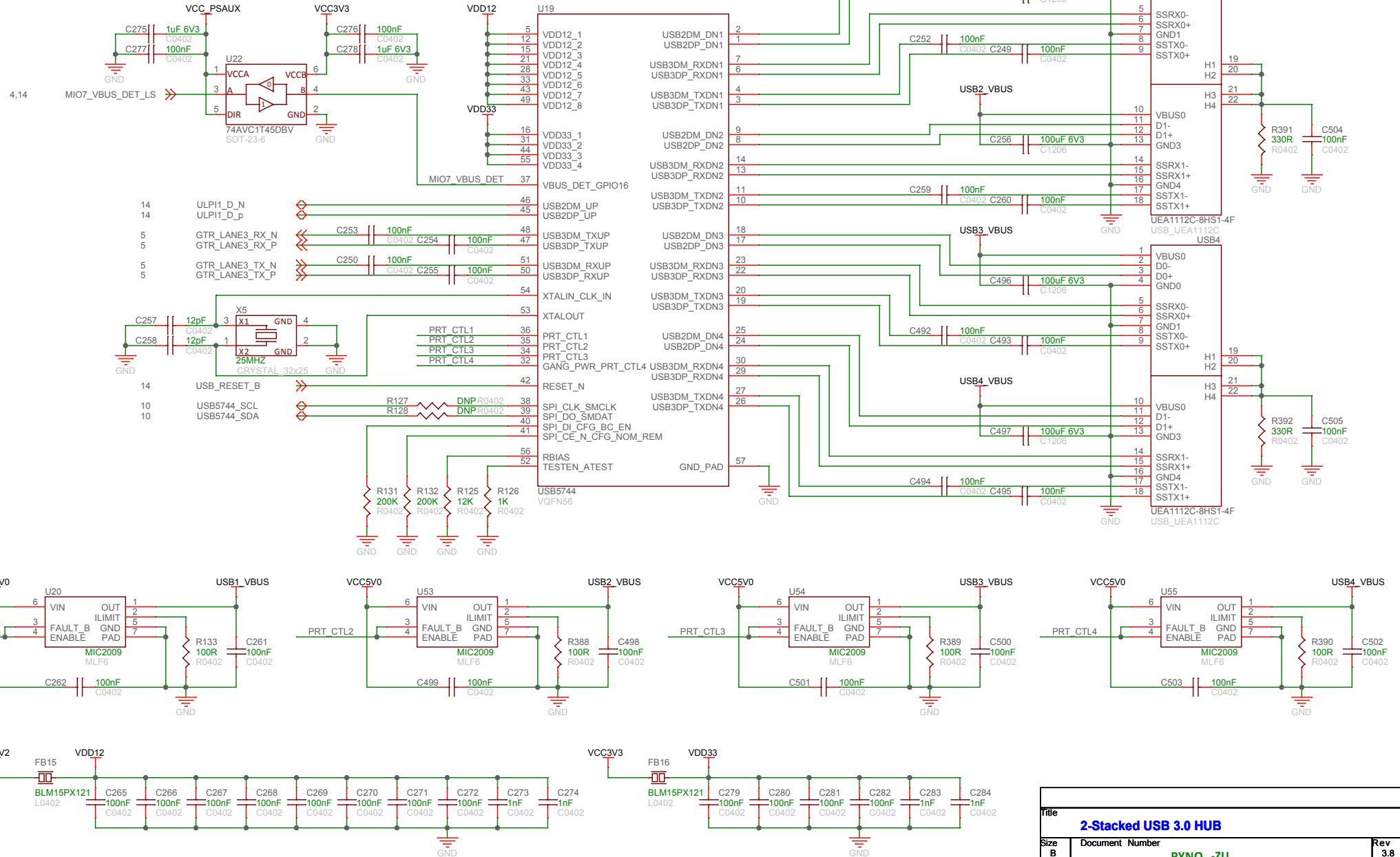
USB 5GHz



Title		
USB Composite device		
Size	Document Number	Rev
B	PYNQ_ZU	3.8
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# PS USB 3.0 HUB

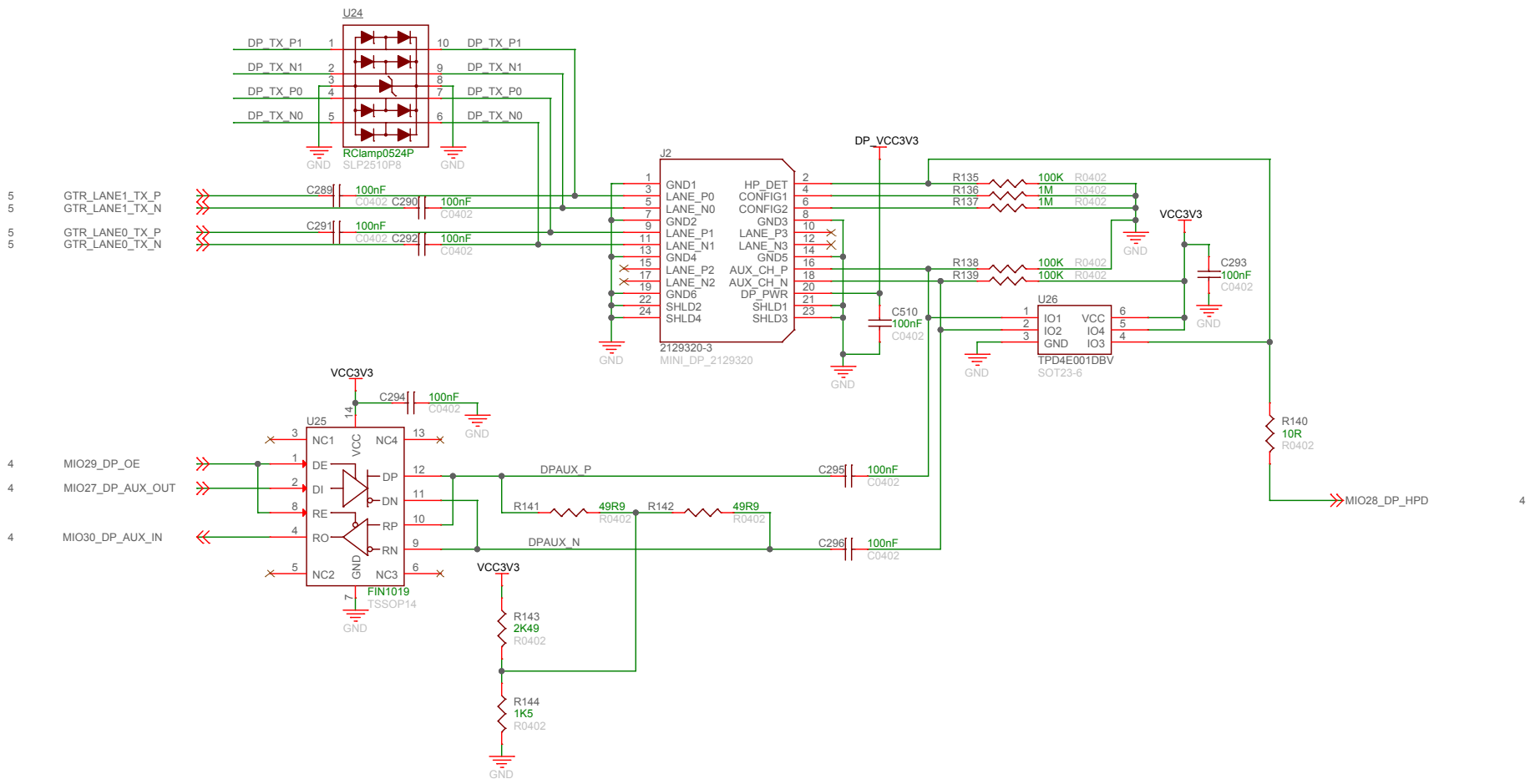
## USB 5GHz



Title			
<b>2-Stacked USB 3.0 HUB</b>			
Size	Document Number	Rev	
B	<b>PYNQ-ZU</b>	3.8	
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# PS Mini Display Port

Mini DP 5.4GHz

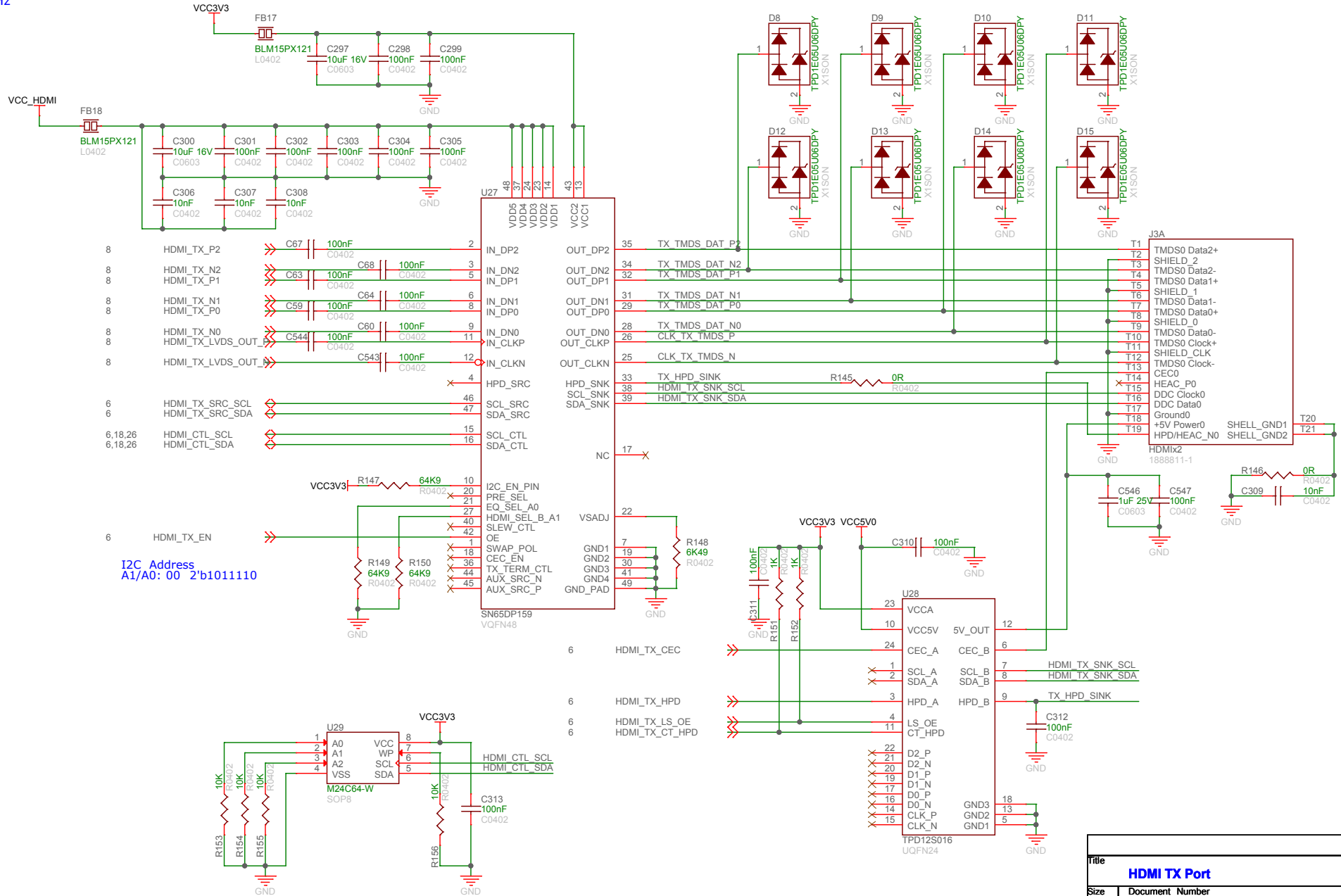


Title		<b>Mini Display port</b>	
Size	Document Number	PYNQ-ZU	
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# PL HDMI TX

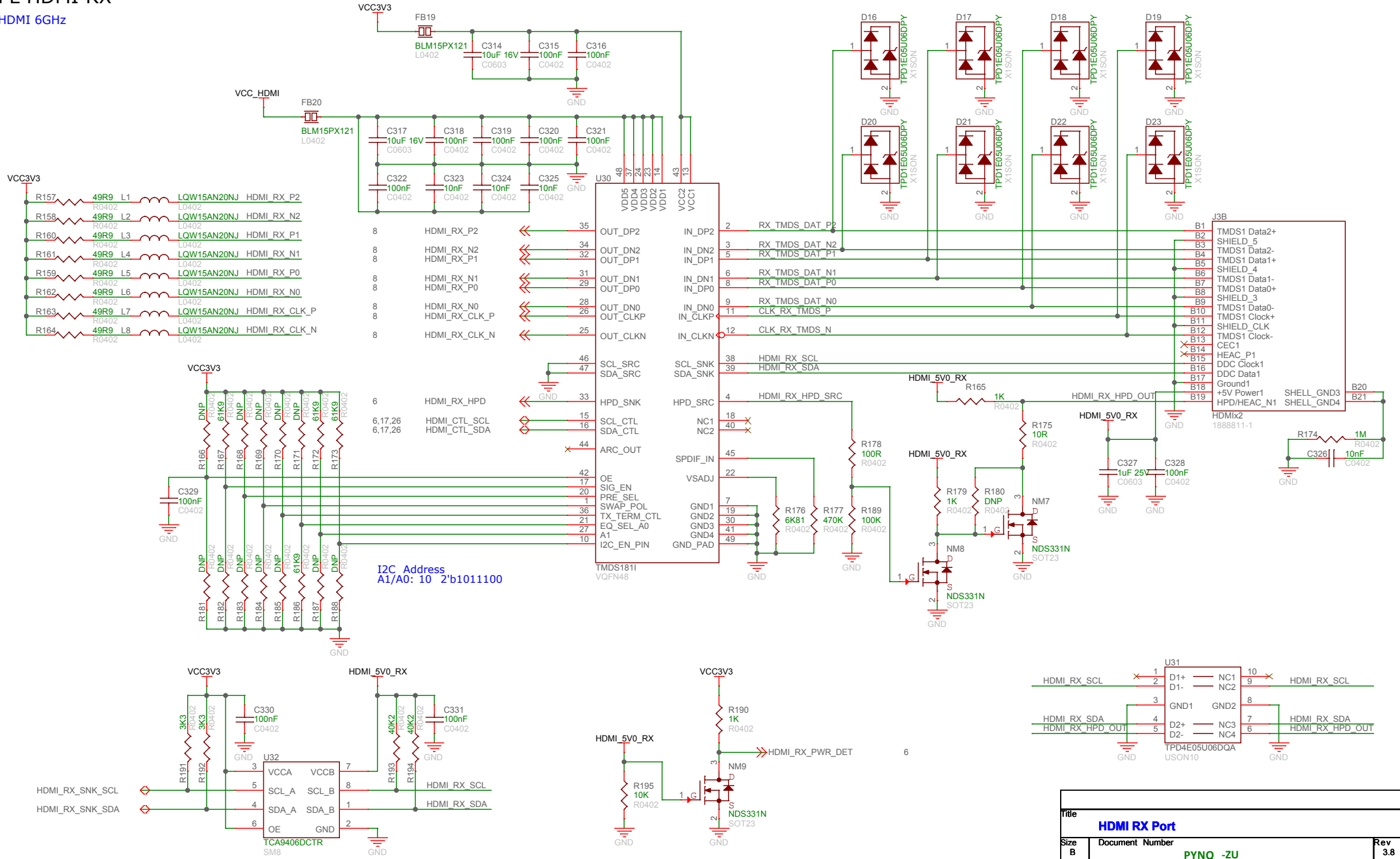
HDMI 6GHz



Title		
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Size	Document Number	Rev
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# PL HDMI RX

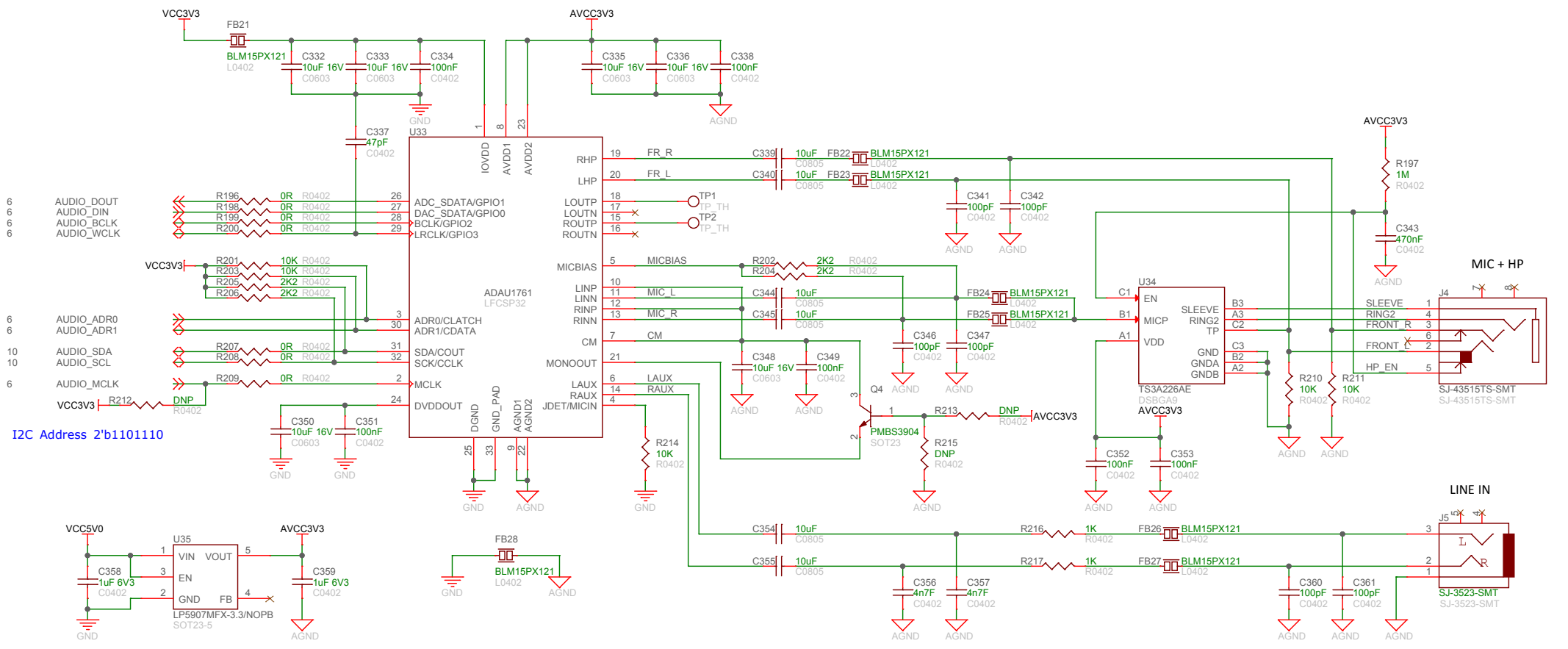
## HDMI 6GHZ



I2C Address  
A1/A0: 10 2'b1011100

Title			
<b>HDMI RX Port</b>			
Size	Document Number	Rev	
B	PYNQ_ZU	3.8	
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# AUDIO & JACK

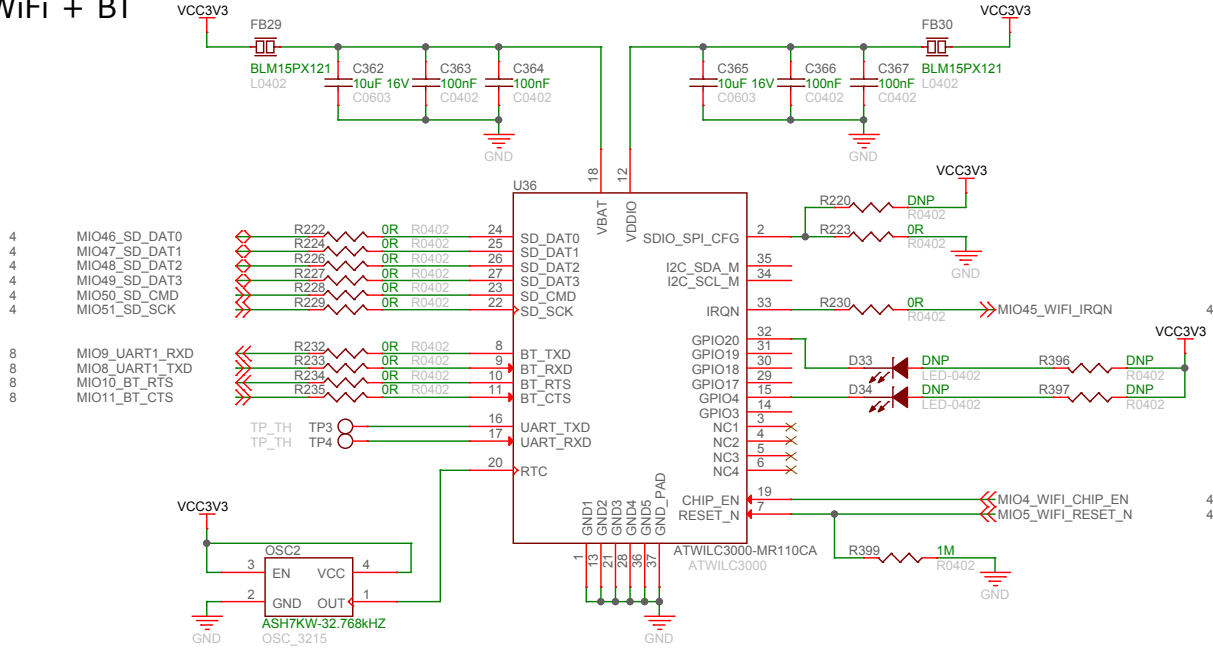


- 6 AUDIO\_DOUT
- 6 AUDIO\_DIN
- 6 AUDIO\_BCLK
- 6 AUDIO\_WCLK
  
- 6 AUDIO\_ADR0
- 6 AUDIO\_ADR1
- 10 AUDIO\_SDA
- 10 AUDIO\_SCL
- 6 AUDIO\_MCLK

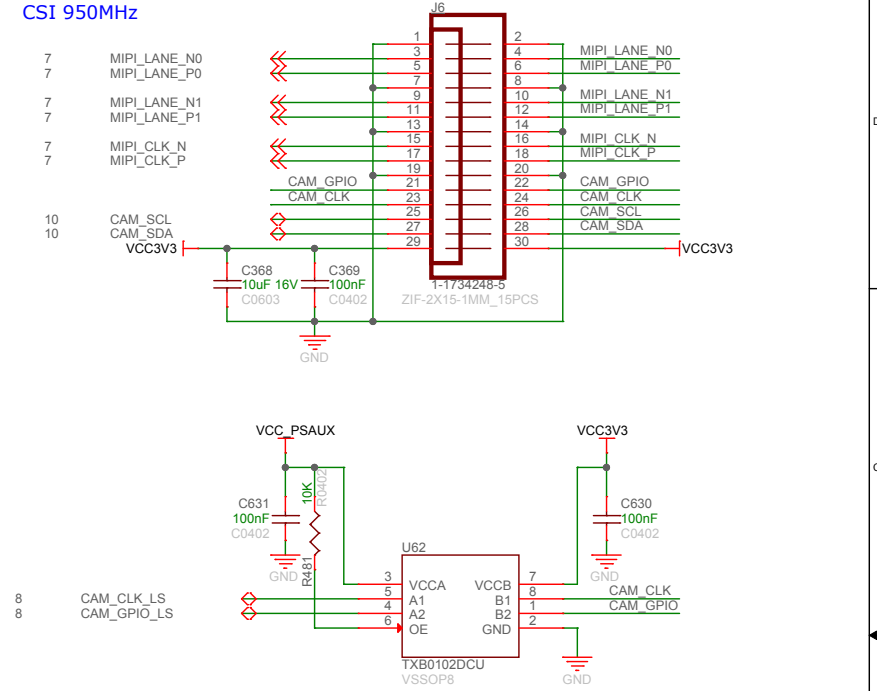
I2C Address 2'b1101110

Title		<b>Audio Codec</b>	
Size	Document Number	PYNQ_ZU	
B			
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			Rev 3.8

# WiFi + BT

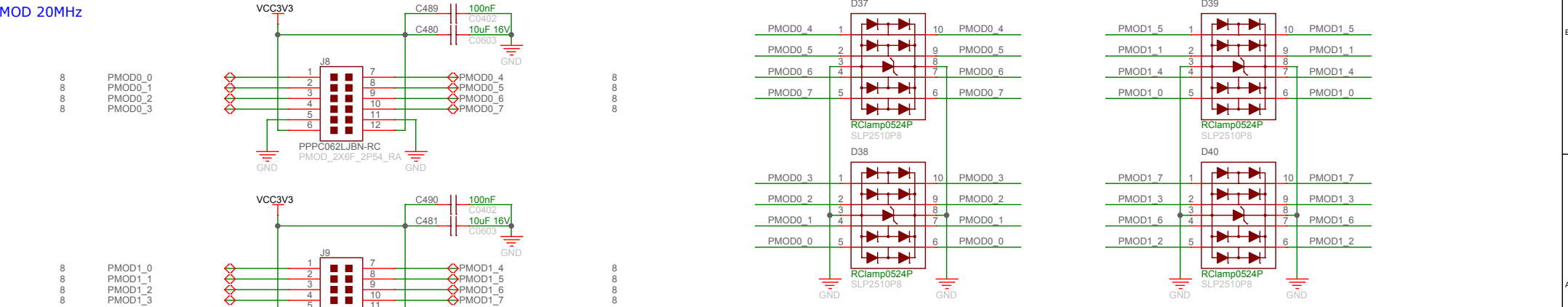


# MIPI CSI



# PMOD

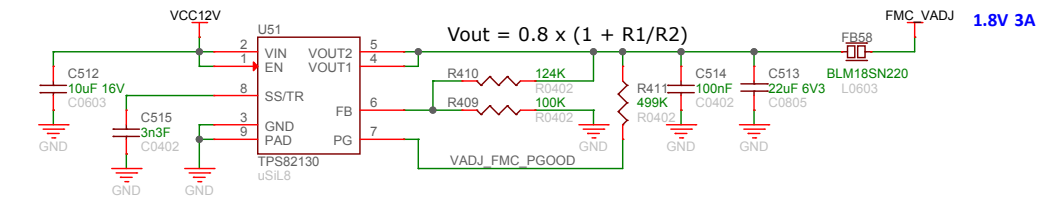
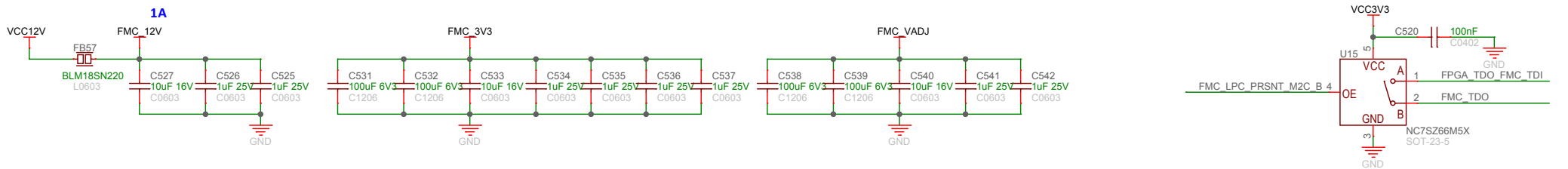
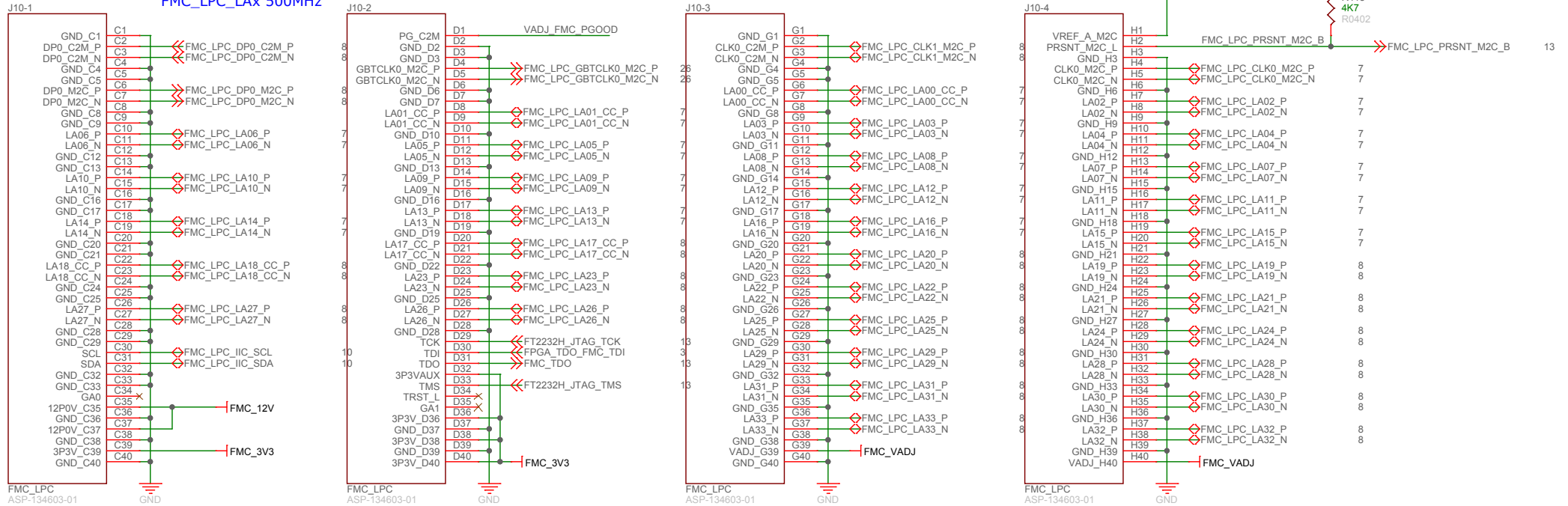
PMOD 20MHz



Title		
<b>WiFi+BT &amp; CSI &amp; Dual PMOD</b>		
Size	Document Number	Rev
B	<b>PYNQ-ZU</b>	3.8
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# FMC LPC Rows C D G H

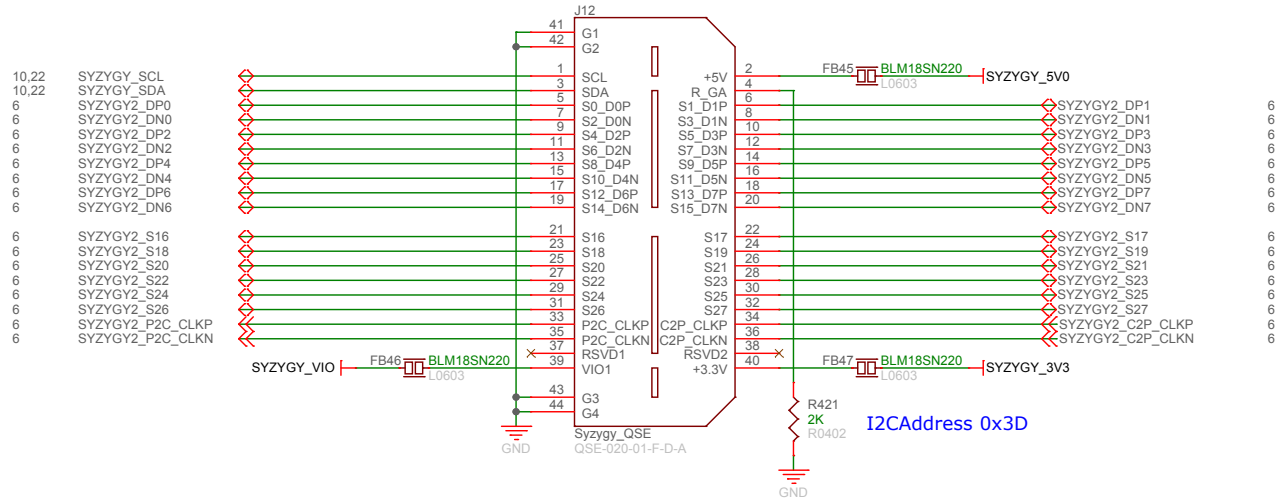
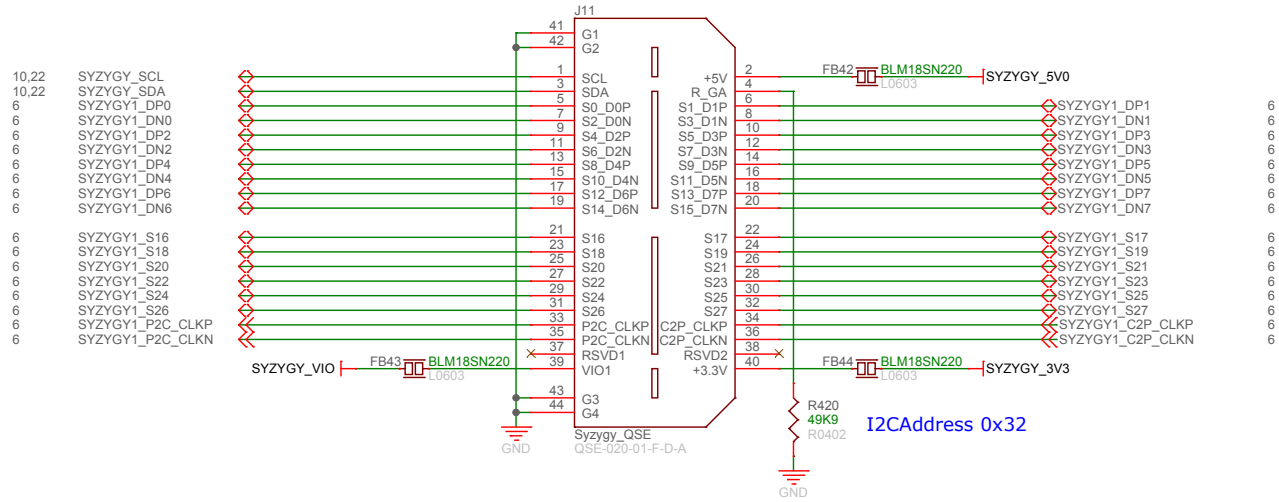
FMC\_LPC\_DP0 5GHz  
FMC\_LPC\_LAx 500MHz



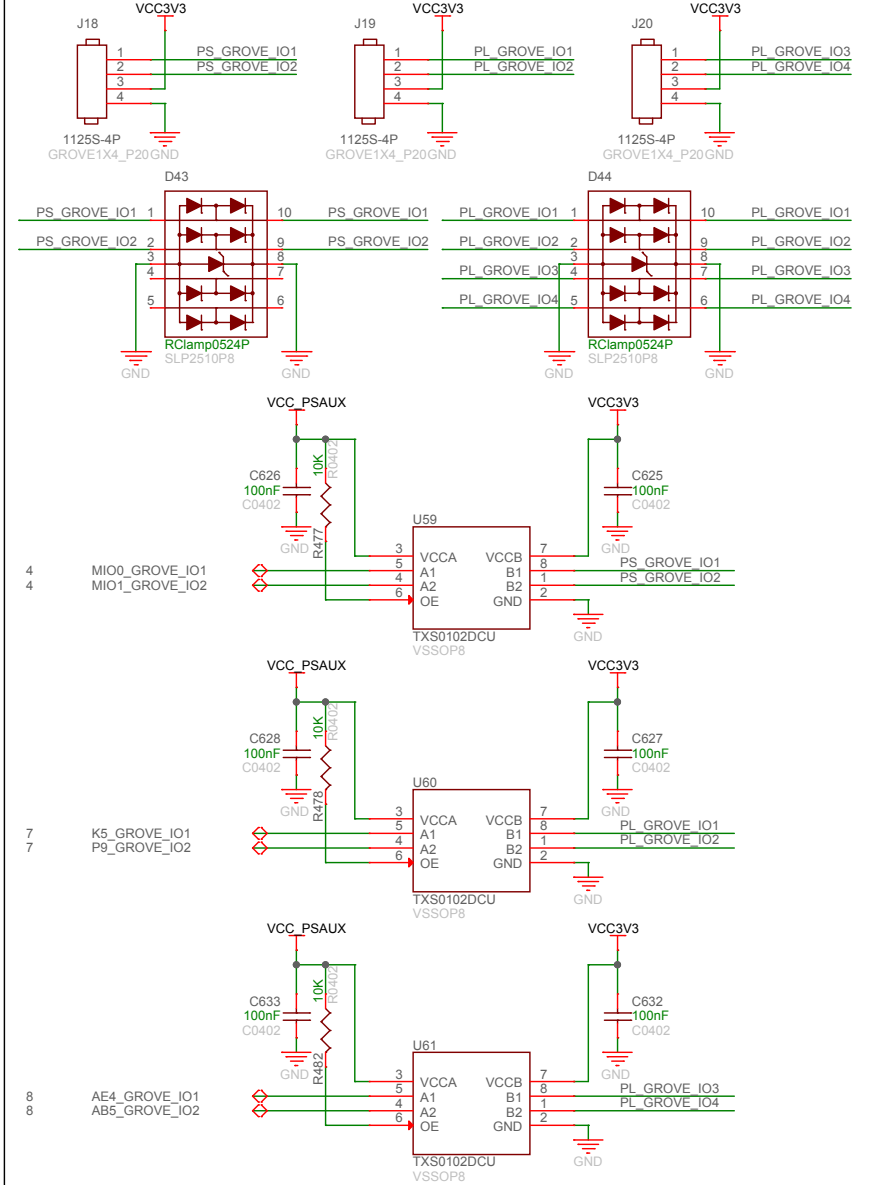
Title			
<b>FMC LPC</b>			
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# Dual SYZYGY Standard Ports

SYZYGY 500MHz



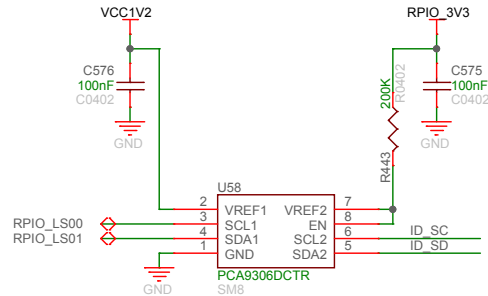
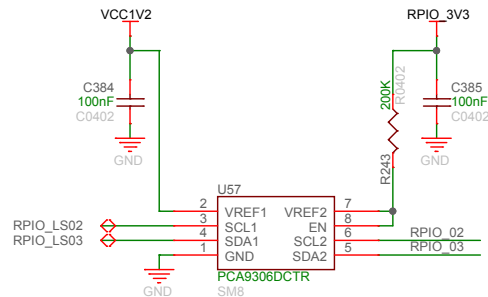
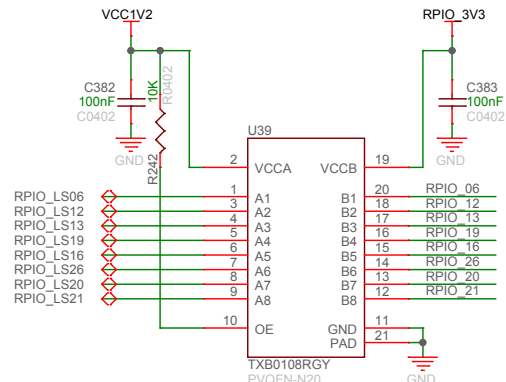
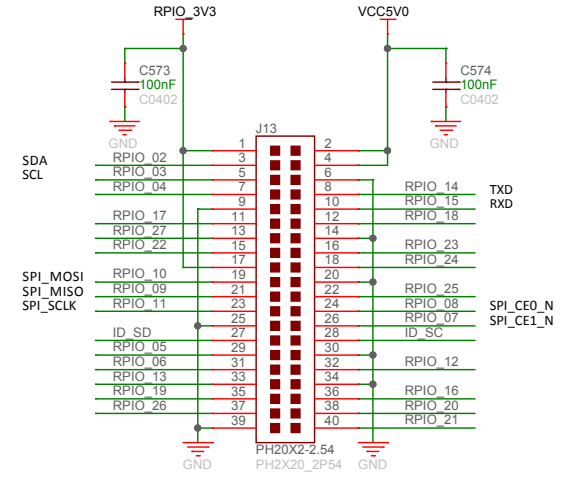
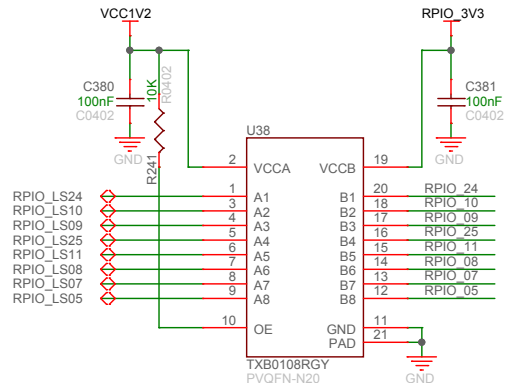
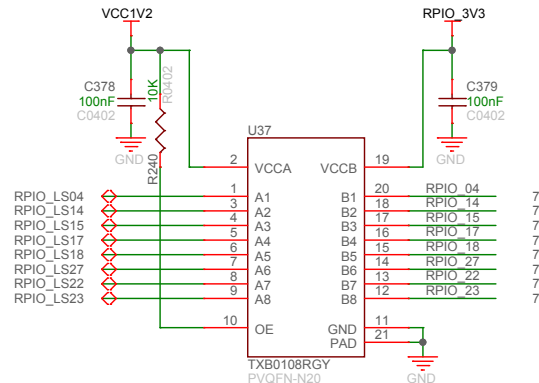
# GROVE Interface



Title			
<b>Dual SYZYGY Standard Ports</b>			
Size	Document Number	Rev	
B	<b>PNYQ_7ZU</b>	3.8	
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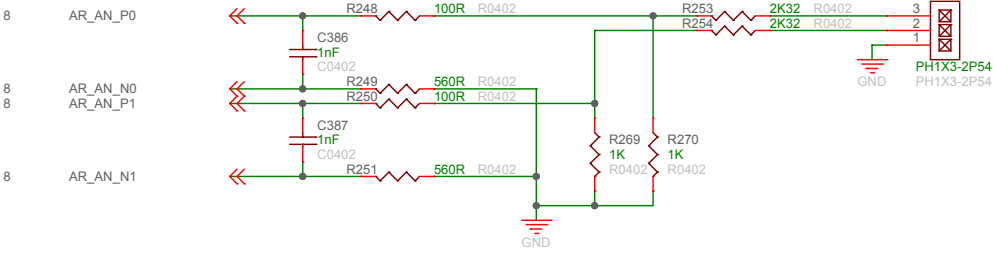
# Raspberry Pi GPIOs

RPI 100MHz



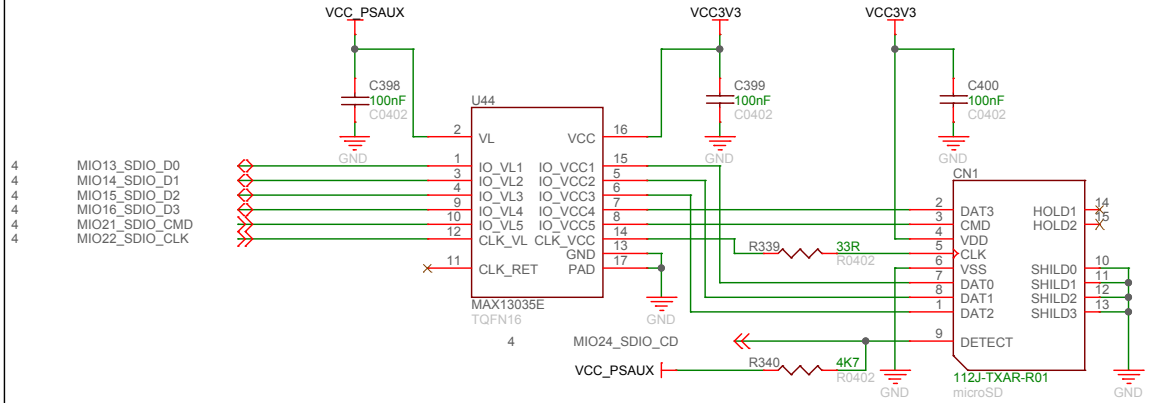
Title		
<b>40-Pin Raspberry Pi GPIOs</b>		
Size B	Document Number	Rev 3.8
	<b>PYNO-ZU</b>	
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## External Analog Inputs

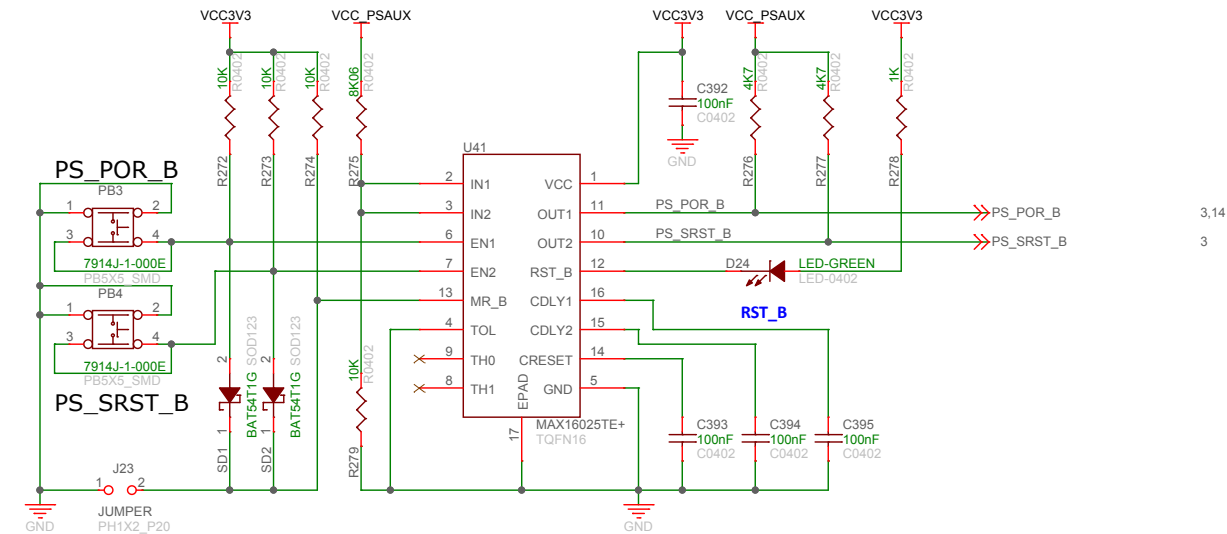


## Micro SD

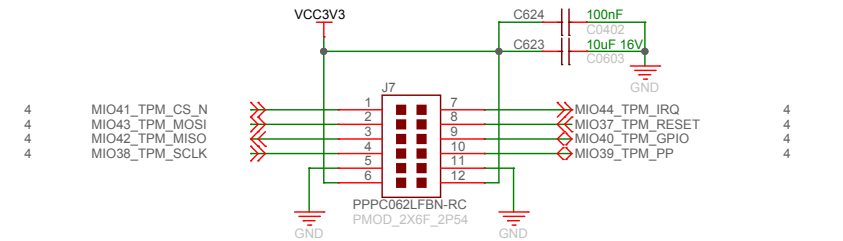
150Mbps



## Supervisory



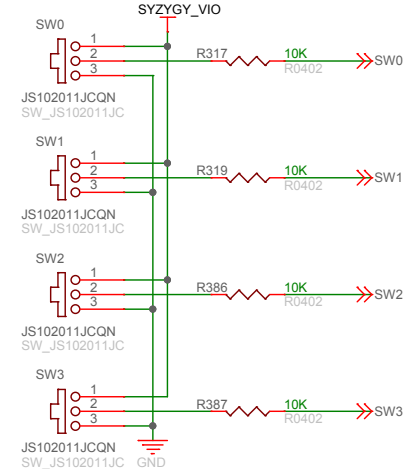
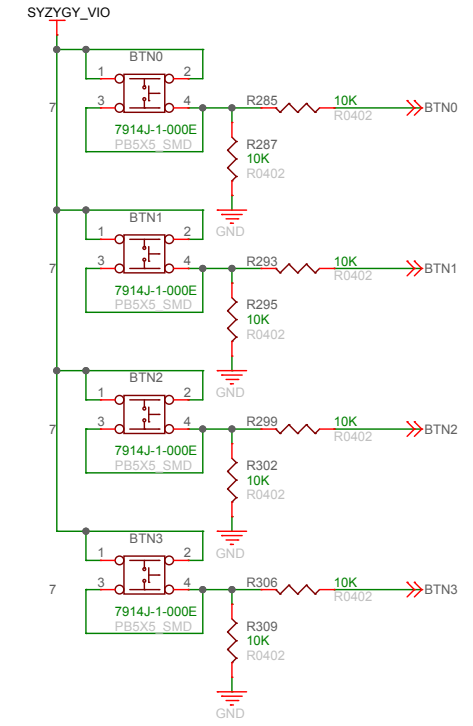
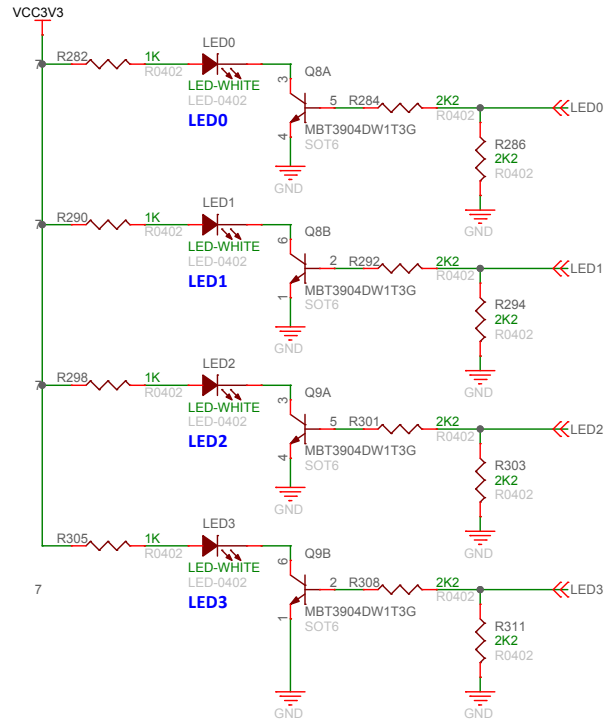
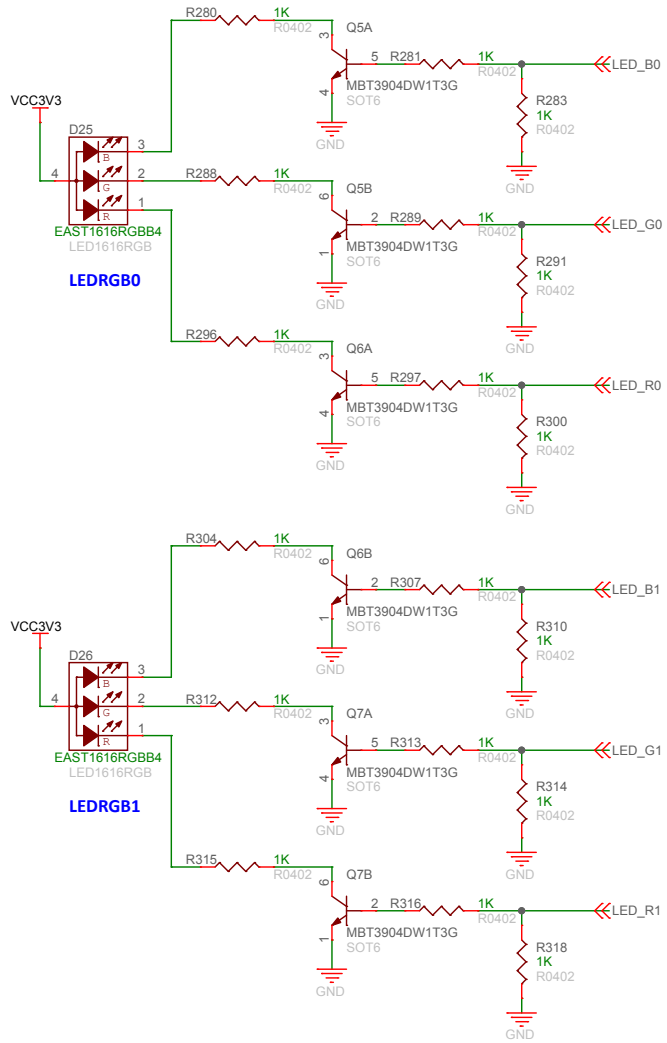
## TPM PMOD



Title		
<b>XADC &amp; Micro SD &amp; TPM PMOD</b>		
Size	Document Number	Rev
B	<b>PYNQ_ZU</b>	<b>3.8</b>
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# Buttons & LEDs

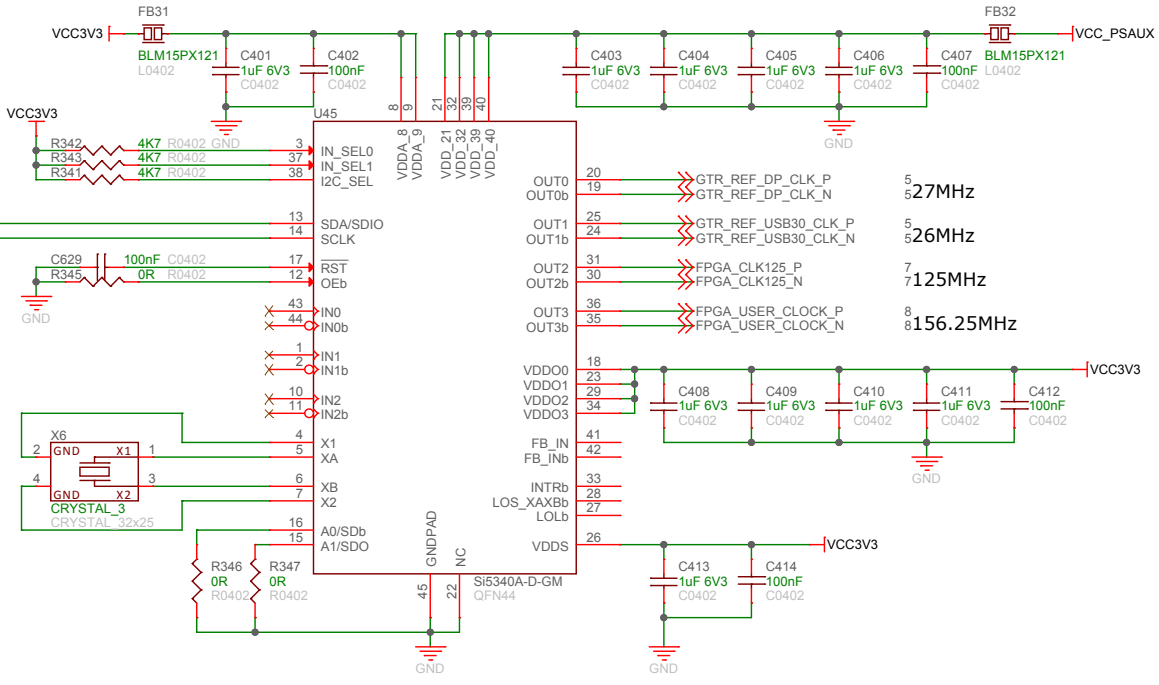


Title		
<b>SWs &amp; LEDs &amp; Push Buttons</b>		
Size	Document Number	Rev
B	<b>PYNQ_ZU</b>	<b>3.8</b>
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# Clock Sources

I2C Address 2'b1110100

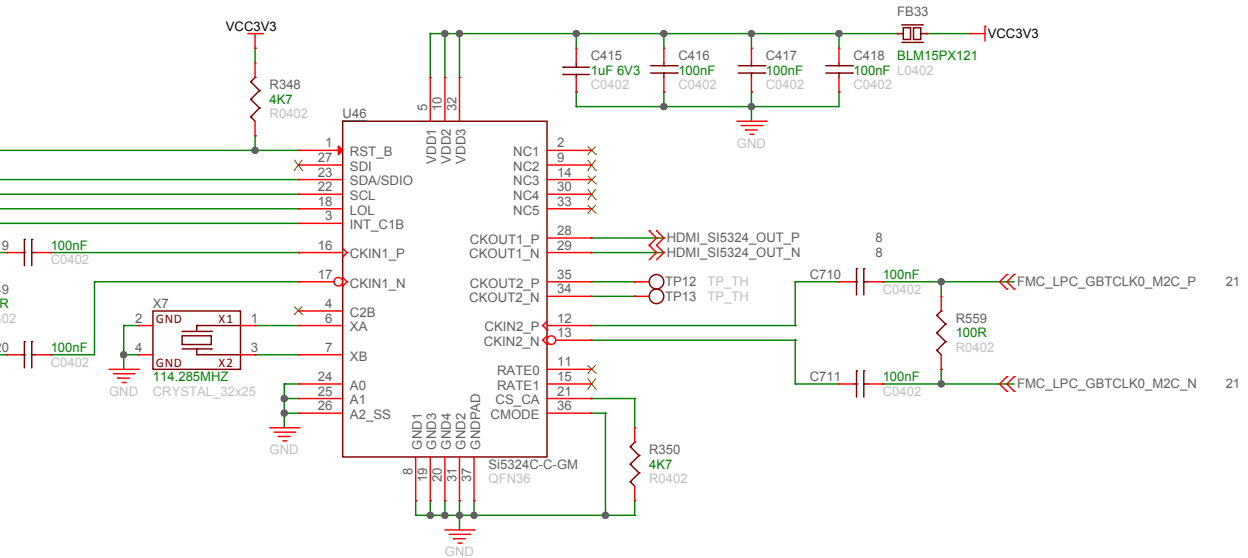
10 SI5340A\_SDA  
10 SI5340A\_SCL



I2C_SEL	Selected I/F	IN_SEL[1:0]	Selected Input
0	SPI	00	IN0
1	I2C	01	IN1
		10	IN2
		11	XA/XB

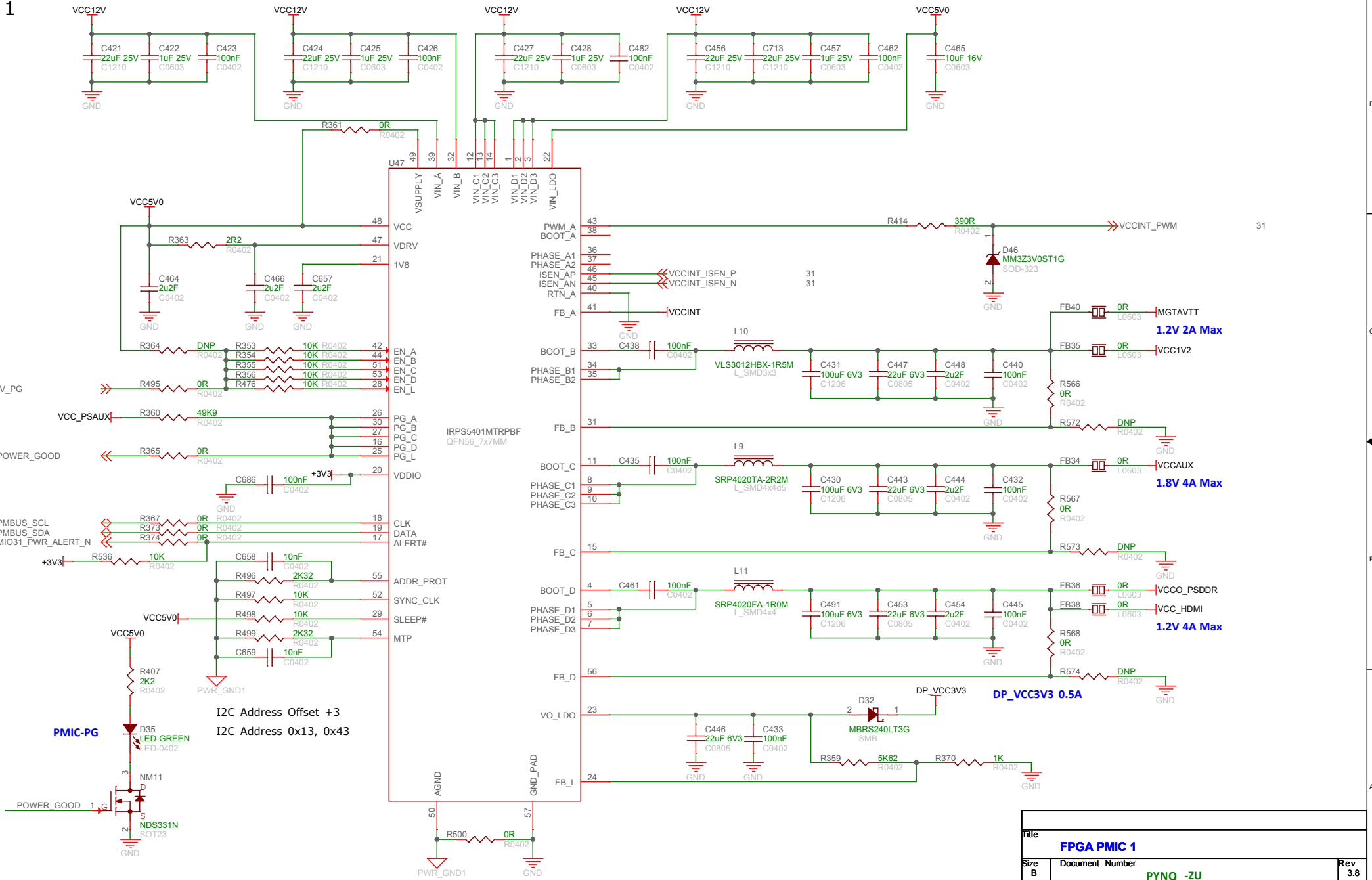
I2C Address 2'b1101000

6 HDMI\_SI5324\_RST  
6,17,18 HDMI\_CTL\_SDA  
6,17,18 HDMI\_CTL\_SCL  
6 HDMI\_SI5324\_LOL  
6 HDMI\_SI5324\_INT\_ALM  
7 HDMI\_REC\_CLOCK\_P  
7 HDMI\_REC\_CLOCK\_N



Title		
Clock Sources		
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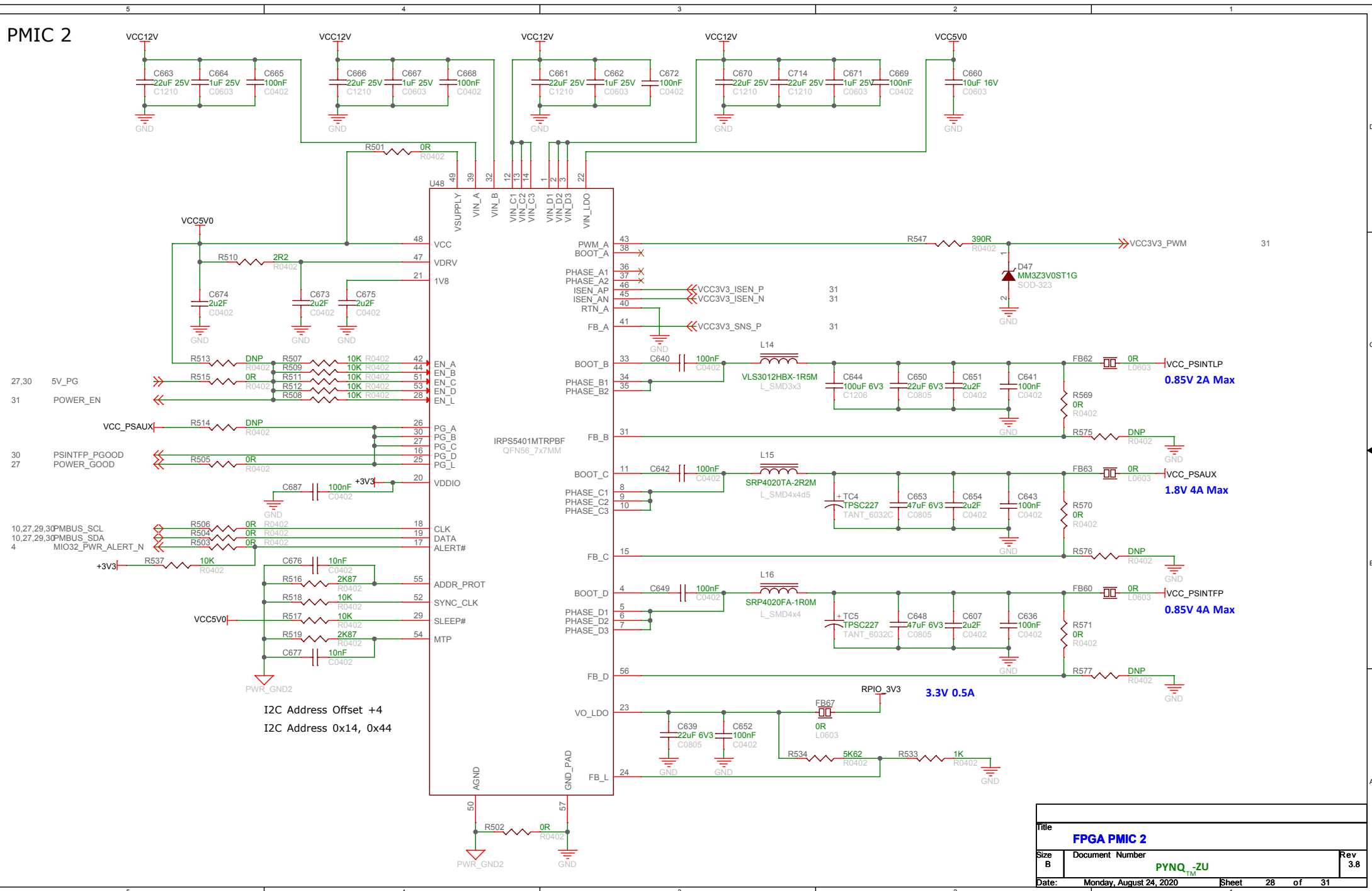
# PMIC 1



I2C Address Offset +3  
I2C Address 0x13, 0x43

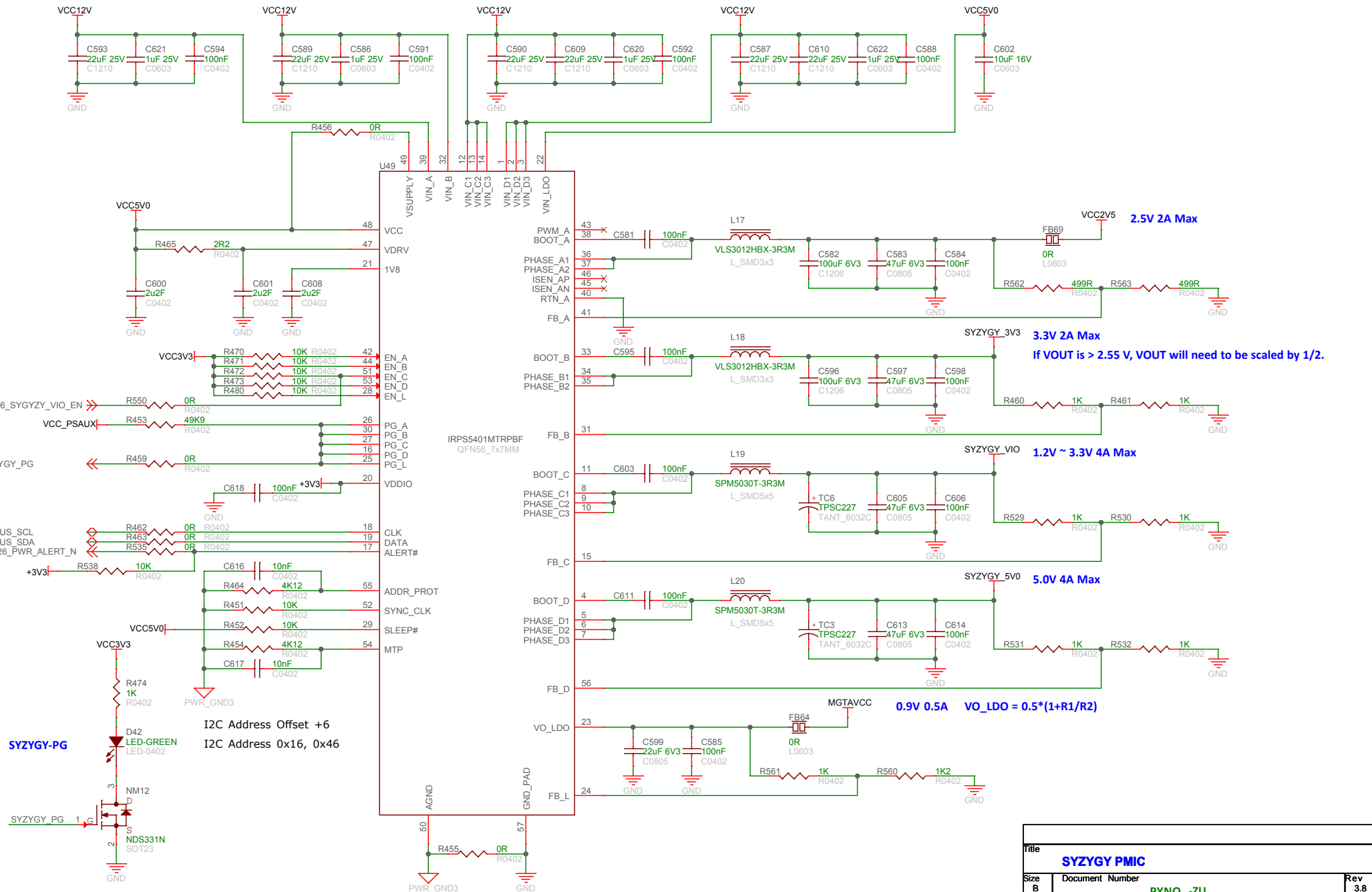
Title			
FPGA PMIC 1			
Size	Document Number	Rev	
B		3.8	
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# PMIC 2



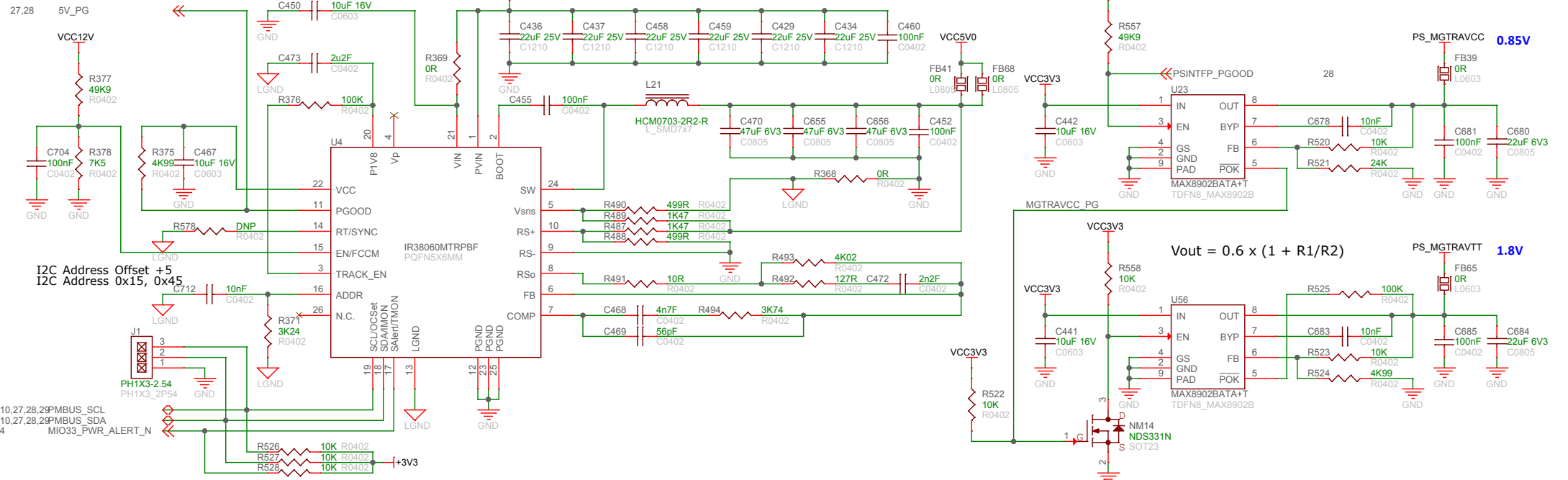
Title		
FPGA PMIC 2		
Size	Document Number	Rev
B	PYNQ_ZU	3.8
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# PMIC 3

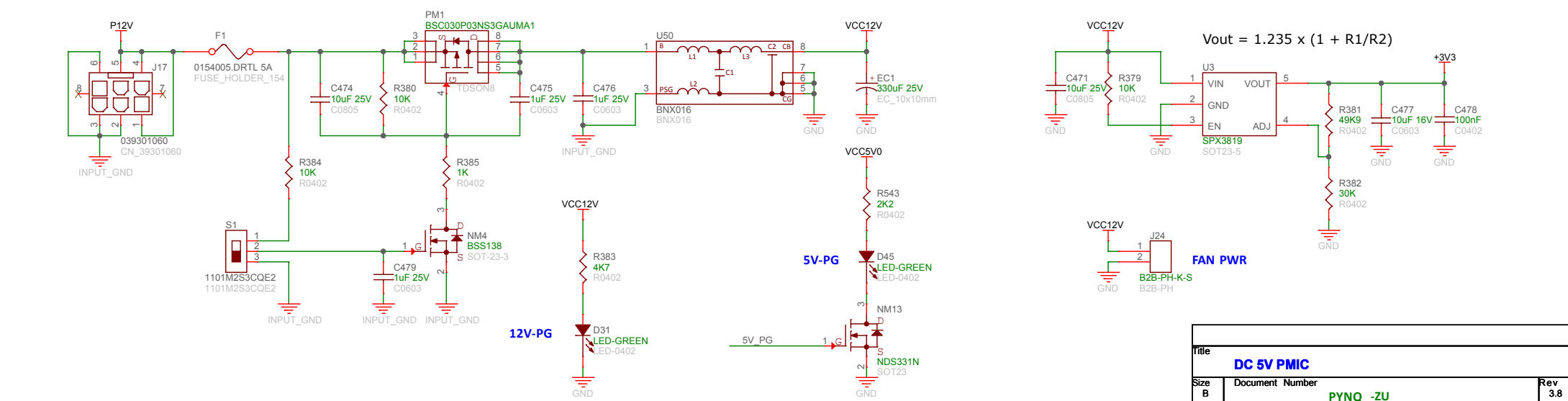


Title		
SYZYGY PMIC		
Size	Document Number	Rev
B	PYNQ_ZU	3.8
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# DC 5V 6A

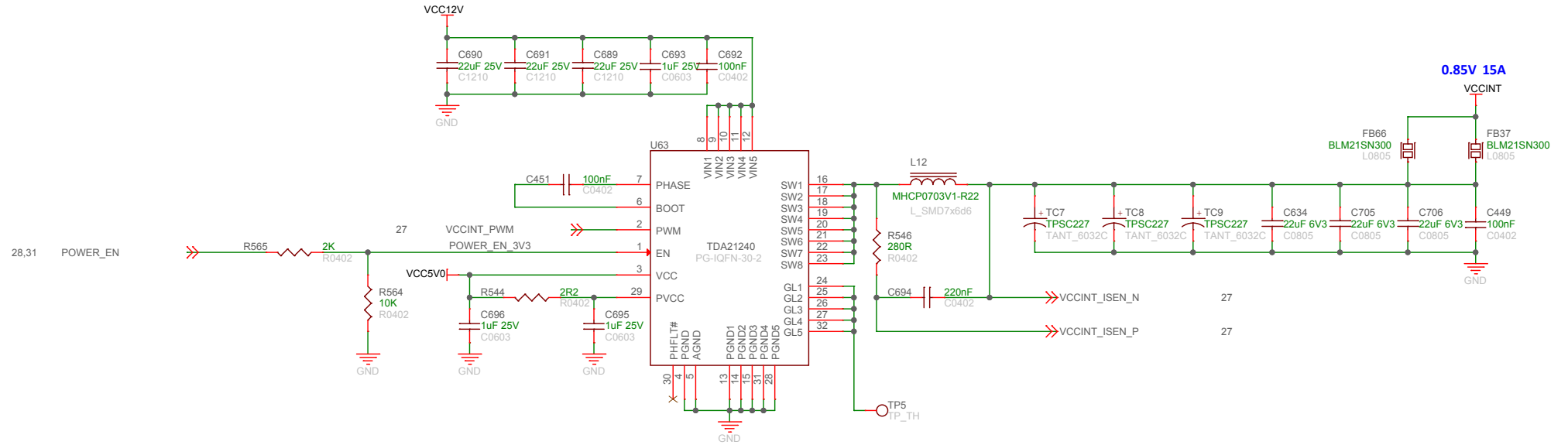


# DC INPUT

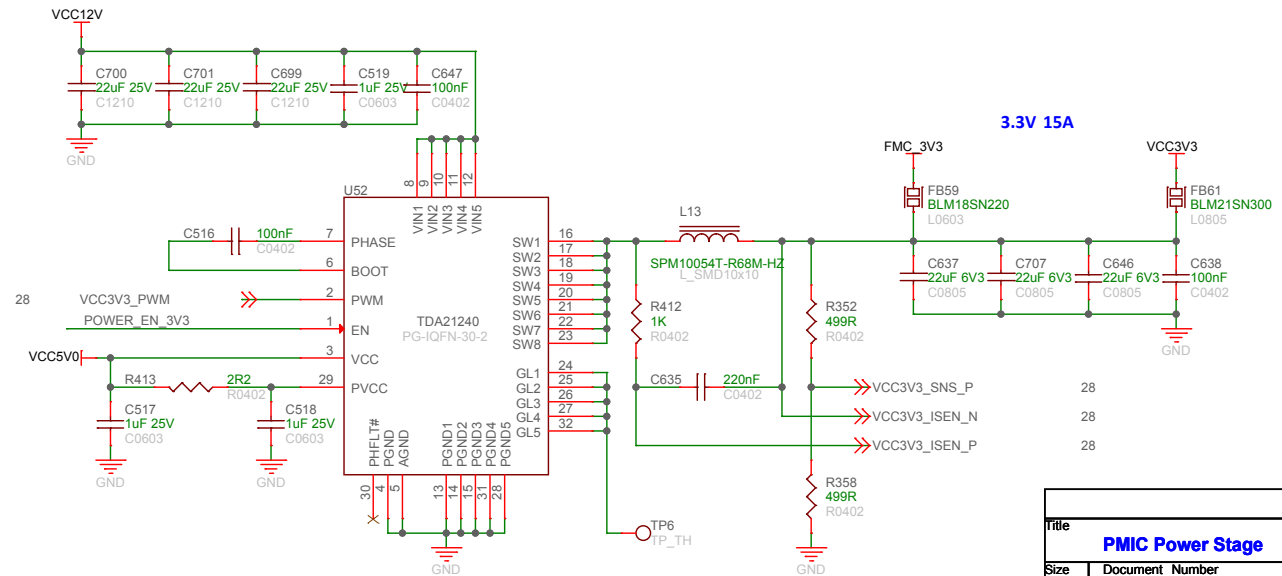


Title			
<b>DC 5V PMIC</b>			
Size	Document Number	Rev	
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# PMIC 1 Power Stage



# PMIC 2 Power Stage



Title			
<b>PMIC Power Stage</b>			
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